SPECIFICATIONS FOR TFT-LCD MODULE

Model Name: DBT034BOIA01

Version：	0

■ Approved For Specifications

□ Approved For Specifications & Sample

APTUS ELECTRONICS CO., LIMITED:

Disea Model No.：	DBT034BOIA01
Prepared by:	Bob
Checked by	Luck
Approved by:	Jack

CUSTOMER:

Customer Model No.:	
Approved by:	
Date：	
Note：	

RECORD OF REVISION

Rev No.	Rev Date	Page	Contents	Editor
V0	2025/1/19		New issue.	Bob

TABLE OF CONTENTS

1. Scope

This specification defines general provisions as well as inspection standards for TFT module supplied by APTUS electronics Co.,LTD.

If the event of unforeseen problem or unspecified items may occur, naturally shall negotiate and agree to solution.

2. General Specifications

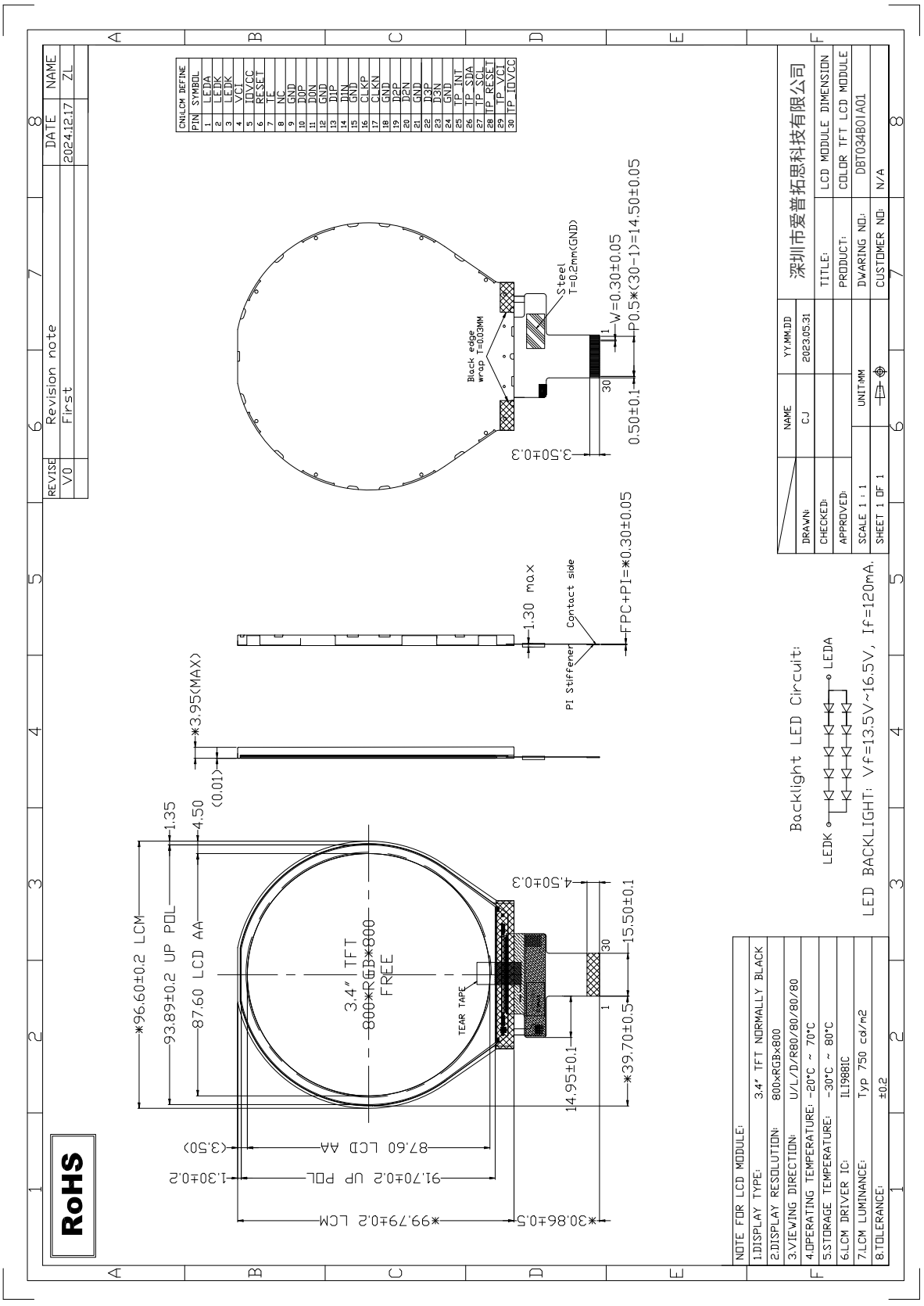
2.1 LCD Parameter

Item	Contents	Unit	Note
LCD Type	TFT	-	
Display color	16.7M		
Viewing Direction	ALL	O'Clock	
Operating temperature	-20~+70	℃	
Storage temperature	-30~+80	℃	
Module size	3.1	inch	
Active Area(W×H)	87.60x87.60	mm	
Number of Dots	800x800	dots	
Controller	ILI9881C	-	
Power Supply Voltage	3.3	V	
Outline Dimensions	96.60x99.79x3.95	mm	
Backlight	5X2-LEDs (white)	pcs	
Weight	---	g	
Interface	MIPI	-	

Note 1: Color tune is slightly changed by temperature and driving voltage.

Note 2: Without FPC and Solder.

3.Outline Drawing



4.Interface Description

4.1 LCD interface

Pin	Symbol	I/O	Function	Note
1	LEDA	P	LED back light(Anode).	
2-3	LEDK	P	LED back light(Cathode).	
4	VCI	P	Analog Power supply.	
5	IOVCC	P	Digital Power supply.	
6	RESET	I	Reset pin, Active Low.	
7	TE	O	Tearing effect output pin.	
8	NC	-	No connect.	
9	GND	P	Ground.	
10	D0P	I	MIPI differential data0+ input.	
11	D0N	I	MIPI differential data0- input..	
12	GND	P	Ground.	
13	D1P	I	MIPI differential data1+ input.	
14	D1N	I	MIPI differential data1- input.	
15	GND	P	Ground.	
16	CLKP	I	MIPI CLOCK+differential signal input .	
17	CLKN	I	MIPI CLOCK- differential signal input.	
18	GND	P	Ground.	
19	D2P	I	MIPI differential data2+ input.	
20	D2N	I	MIPI differential data2- input.	
21	GND	P	Ground.	
22	D3P	I	MIPI differential data3+ input.	
23	D3N	I	MIPI differential data3-input.	
24	GND	P	Ground.	
25	TP_INT (NC)	I	External Interrupt to the IC of CTP.	
26	TP_SDA (NC)	I/O	CTP Serial in/out signal pin.	
27	TP_SCL (NC)	I	CTP Serial interface clock pin.	
28	TP_RESET (NC)	I	CTP Reset pin.	
29	TP_VCI (NC)	P	CTP Analog or digital supply voltage.	
30	TP_IOVCC (NC)	P	CTP I/O circuit or logic supply voltage.	

5. Absolute Maximum Ratings(Ta=25℃)

5.1 Electrical Absolute Maximum Ratings.(Vss=0V ,Ta=25℃)

Item	Symbol	Min.	Max.	Unit	Note
Power Supply Voltage	VCI	-0.3	7.0	V	1，2
	IOVCC	-0.3	3.8		
	VGH	-0.3	+18		
	VGL	-18	-0.3		

Notes:

1. If the module is above these absolute maximum ratings. It may become permanently damaged. Using the module within the following electrical characteristic conditions are also exceeded, the module will malfunction and cause poor reliability.
2. V_{DD} >V_{SS} must be maintained.

5.2 Environmental Absolute Maximum Ratings.

Item	Storage		Operating		Note
	MIN.	MAX.	MIN.	MAX.	
Ambient Temperature	-30℃	80℃	-20℃	70℃	1,2
Humidity	-	-	-	-	3

1. The response time will become lower when operated at low temperature.
2. Background color changes slightly depending on ambient temperature.

   The phenomenon is reversible.
3. Ta<=40℃:85%RH MAX.

   Ta>=40℃:Absolute humidity must be lower than the humidity of 85%RH at 40℃.

6. Electrical Specifications and Instruction Code

6.1 Electrical characteristics(Vss=0V ,Ta=25℃)

Parameter		Symbol	Condition	Min	Typ	Max	Unit	Note
Power supply		VCI	Ta=25℃	2.5	2.8	6.6		
		IOVCC		1.65	1.8	3.6	V	-
Input voltage	'H'	V_{IH}	VDD=3.3V	0.7_{IOVCC}	-	IOVCC	V	-
	'L'	V_{IL}		-0.3	-	0.3_{IOVCC}	V	-
Output voltage	'H'	V_{OH}	IOH= -1.0mA	0.8_{IOVCC}	-	IOVCC	V	-
	'L'	V_{OL}	IOL= +1.0mA	0	-	0.2_{IOVCC}	V	-
Current Consumption		I_{CC}	Ta=25℃	-		-	mA	2
		I_{IOVCC}		-		-	uA	2

Note:

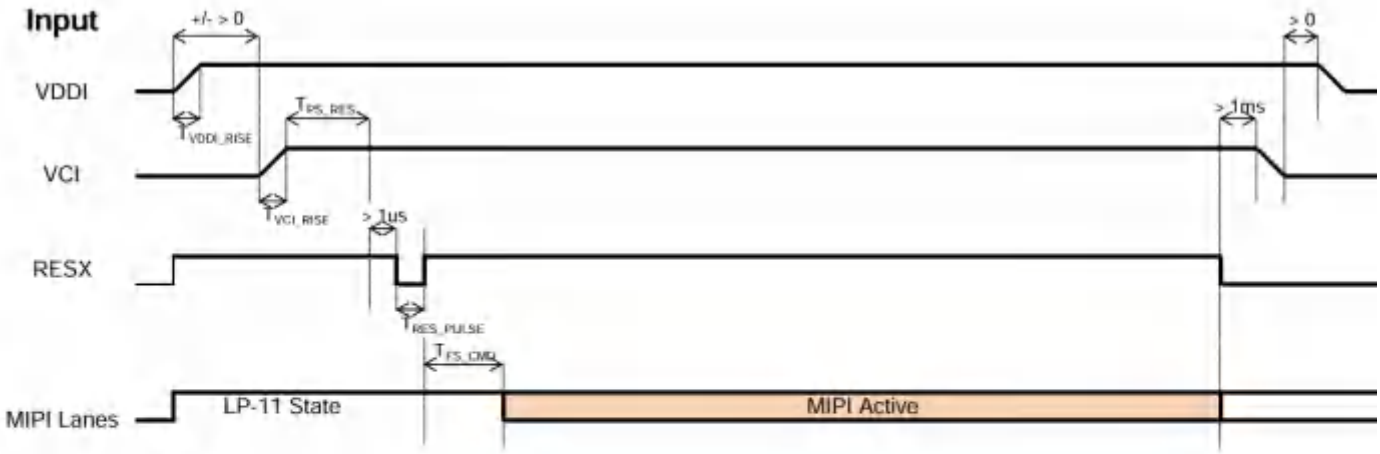
1:When an optimum contrast is obtained in transmissive mode.

2: Tested in 1╳1 chessboard pattern.

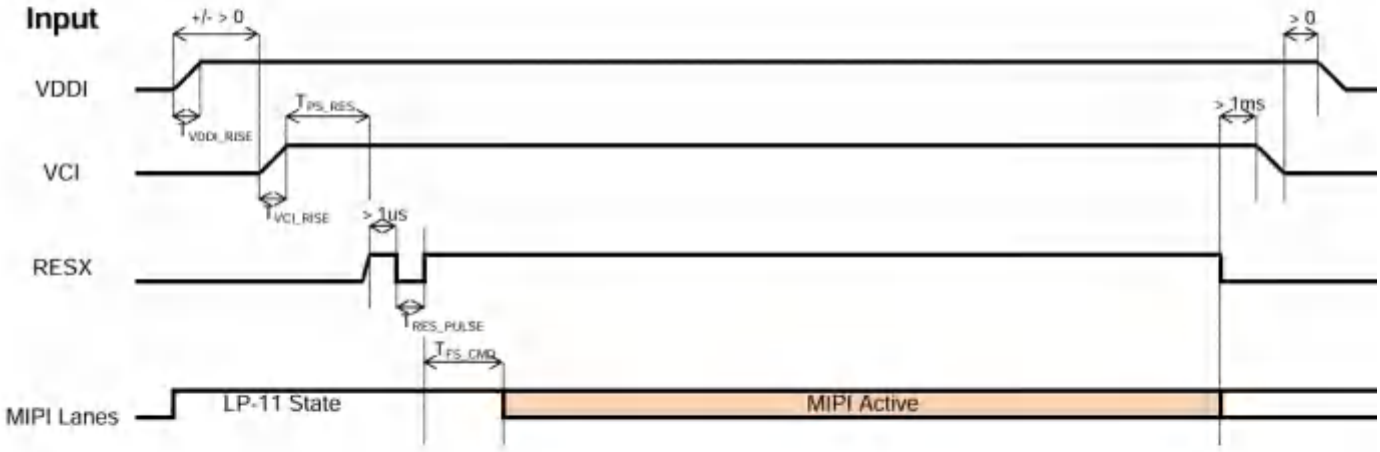
7. Timing Characteristics

7.1 POWER ON/OFF SEQUENCE

Case A:



Case B:



Symbol	Characteristics	Min.	Typ.	Max.	Units
T_{VDDI_RISE}	VDDI Rise time	10	-	-	us
T_{VCI_RISE}	Case A: VCI Rise time	130	-	-	us
	Case B: VCI Rise time	40			
T_{PS_RES}	VDDI/VCI on to Reset high	5	-	-	ms
T_{RES_PULSE}	Reset low pulse time	10	-	-	us
T_{FS_CMD}	Reset to first command	10	-	-	ms

Figure 105: Power on/off sequence with Power Mode 3

7.2 MIPI Interface Characteristics

7.2.1 DSI Timing Characteristics

High Speed Mode – Clock Channel Timing

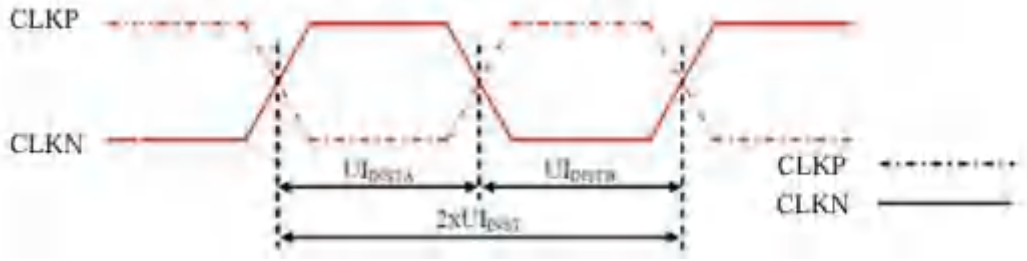


Figure : DSI Clock Channel Timing

Table:DSI Clock Channel Timing

Signal	Symbol	Parameter	Min	Max	Unit
CLKP/N	$2xUI_{INST}$	Double UI instantaneous	*Note 2*	25	ns
CLKP/N	UI_{INSTA}, UI_{INSTB} (Note 1)	UI instantaneous Half	*Note 2*	12.5	ns

Notes:

1. UI = UIINSTA = UIINSTB

2. Define the minimum value, see Table 39.

Table:Limited Clock Channel Speed

Data type	Two Lanes Speed	Three Lanes speed	Four Lanes speed
Data Type = 00 1110 (0Eh), RGB 565, 16 UI per Pixel	566 Mbps	486 Mbps	366 Mbps
Data Type = 01 1110 (1Eh), RGB 666, 18 UI per Pixel	637 Mbps	525 Mbps	472 Mbps
Data Type = 10 1110 (2Eh), RGB 666 Loosely, 24 UI per Pixel	850 Mbps	700 Mbps	550 Mbps
Data Type = 11 1110 (3Eh), RGB 888, 24 UI per Pixel	850 Mbps	700 Mbps	550 Mbps

7.2.2 High Speed Mode-Data Clock Channel Timing

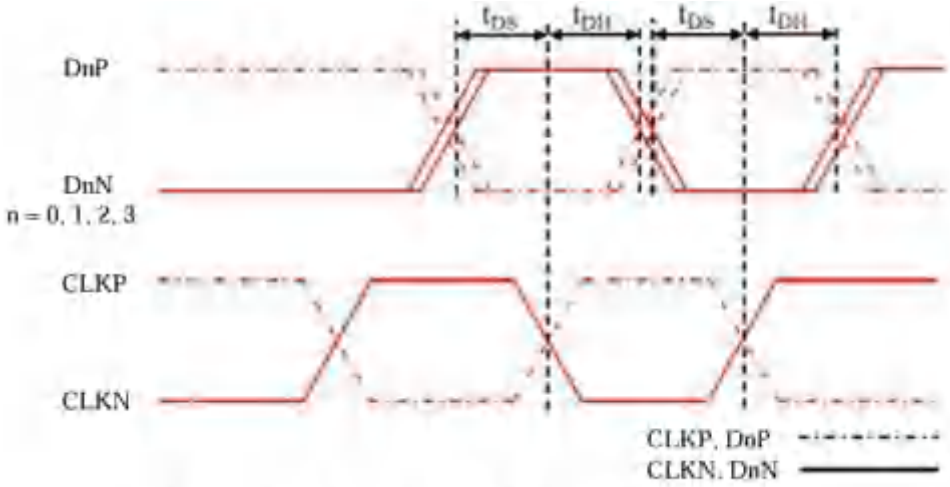


Figure 117: DSI Data to Clock Channel Timings

Table 40: DSI Data to Clock Channel Timings

Signal	Symbol	Parameter	Min	Max
DnP/N , n=0,1,2,3	t_{DS}	Data to Clock Setup time	0.15xUI	-
	t_{DH}	Clock to Data Hold Time	0.15xUI	-

7.2.3 High Speed Mode - Rising and Falling Timings

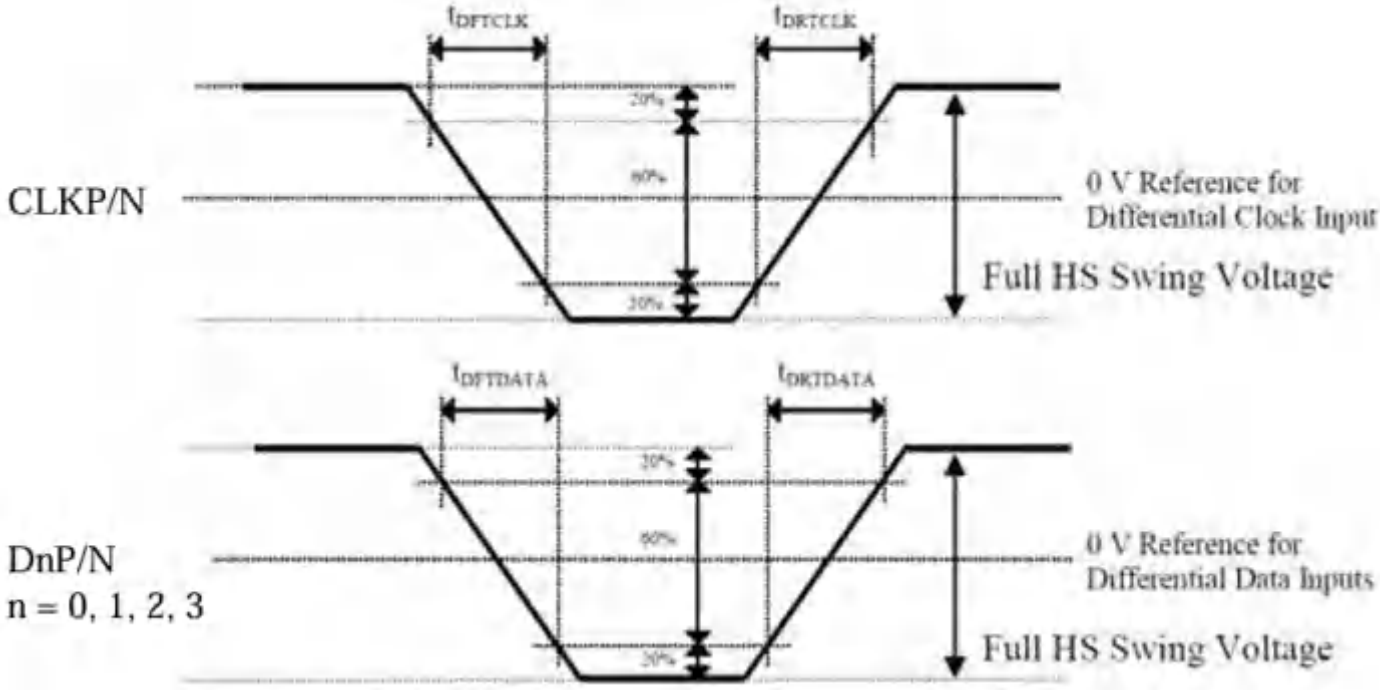


Table:Rise and Fall Timings on Clock and Data Channels

Parameter	Symbol	Condition	Specification		
			Min	Typ	Max
Differential Rise Time for Clock	t_{DRTCLK}	CLKP/N	150 ps	-	0.3UI (Note)
Differential Rise Time for Data	$t_{DRTDATA}$	DnP/N n=0,1,2,3	150 ps	-	0.3UI (Note)
Differential Fall Time for Clock	t_{DFTCLK}	CLKP/N	150 ps	-	0.3UI (Note)
Differential Fall Time for Data	$t_{DFTDATA}$	DnP/N n=0,1,2,3	150 ps	-	0.3UI (Note)

Note: *The display module has to meet timing requirements, which are defined for the transmitter (MCU) on MIPI D-Phy standard.*

7.2.4 Low Speed Mode-Bus Turn Around

Lower Power Mode and its State Periods on the Bus Turnaround (BTA) from the MCU to the Display Module (ILI9881C-0H) are illustrated for reference purposes below.

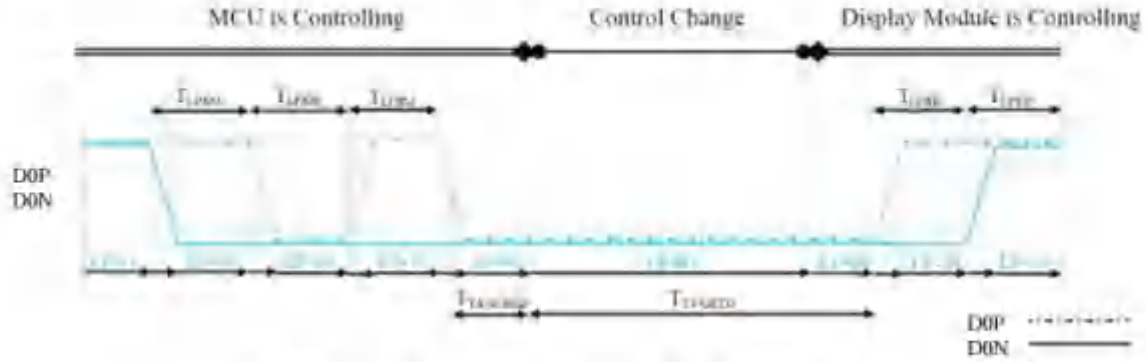


Figure 119: BTA from the MCU to the Display Module

Lower Power Mode and its State Periods on the Bus Turnaround (BTA) from the Display Module (ILI9881C-0H) to the MCU are illustrated for reference purposes below.

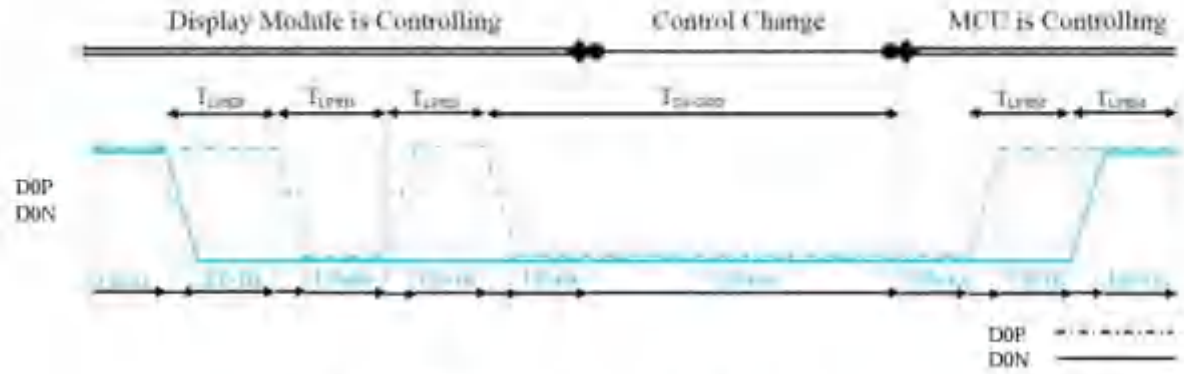


Figure 120: BTA from the Display Module to the MCU

Table 42: Low Power State Period Timings – A

Signal	Symbol	Description	Min	Max	Unit
D0P/N	T_{LPXM}	Length of LP-00, LP-01, LP-10 or LP-11 periods MCU → Display Module (ILI9881C-0H)	50	75	ns
D0P/N	T_{LPXD}	Length of LP-00, LP-01, LP-10 or LP-11 periods Display Module (ILI9881C-0H) → MCU	50	75	ns
D0P/N	$T_{TA\text{-}SURED}$	Time-out before the Display Module (ILI9881C-0H) starts driving	T_{LPXD}	$2xT_{LPXD}$	ns

Table 43: Low Power State Period Timings – B

Signal	Symbol	Description	Time	Unit
D0P/N	$T_{TA\text{-}SETD}$	Time to drive LP-00 by Display Module (ILI9881C-0H)	$5xT_{LPXD}$	ns
D0P/N	$T_{TA\text{-}GOD}$	Time to drive LP-00 after turnaround request - MCU	$4xT_{LPXD}$	ns

7.2.5 Data Lanes from Low Power Mode to High Speed Mode

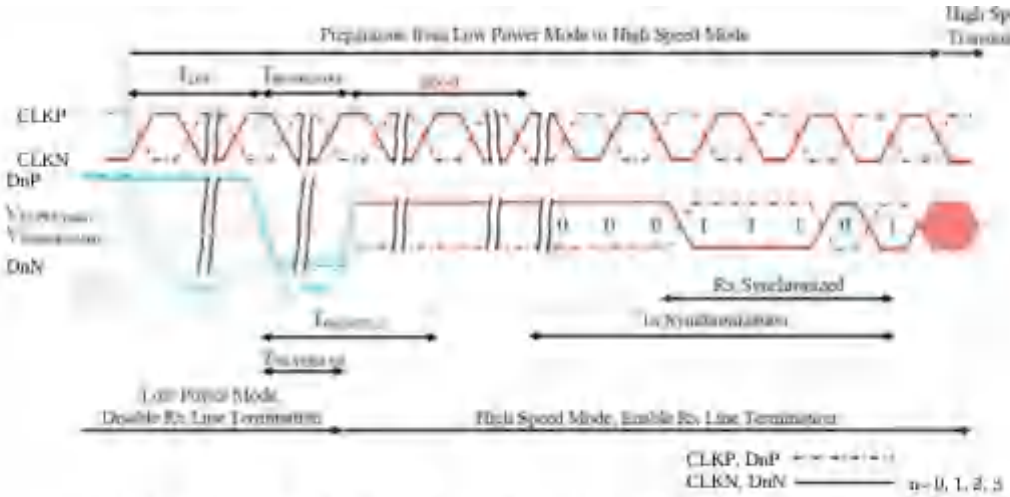


Figure 121: Data Lanes - Low Power Mode to High Speed Mode Timings

Table 44: Data Lanes - Low Power Mode to High Speed Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DnP/N, n = 0,1,2,3	T_{LPX}	Length of any Low Power State Period	50	-	ns
DnP/N, n = 0,1,2,3	$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS Transmission	40+4xUI	85+6xUI	ns
DnP/N, n = 0,1,2,3	$T_{HS-TERM-EN}$	Time to enable Data Lane Receiver line termination measured from when Dn crosses VILMAX	-	35+4xUI	ns

7.2.6 Data Lanes from High Speed Mode to Low Power Mode

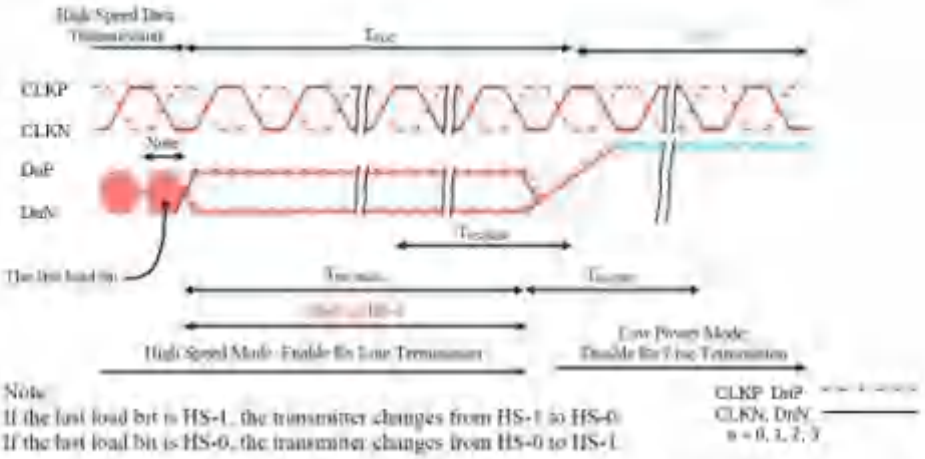


Figure 122: Data Lanes - High Speed Mode to Low Power Mode Timings

Table 45: Data Lanes - High Speed Mode to Low Power Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DnP/N, n = 0,1,2,3	$T_{HS-SKIP}$	Time-Out at Display Module (ILI9881C-0H) to ignore transition period of EoT	40	55+4xUI	ns
DnP/N, n = 0,1,2,3	$T_{HS-EXIT}$	Time to driver LP-11 after HS burst	100	-	ns
DnP/N, n = 0,1,2,3	$T_{HS-TRAIL}$	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst.	Max(8*UI,60ns+4*UI)	-	ns

7.2.7 DSI Clock Burst-High Speed Mode to/from Low Power Mode

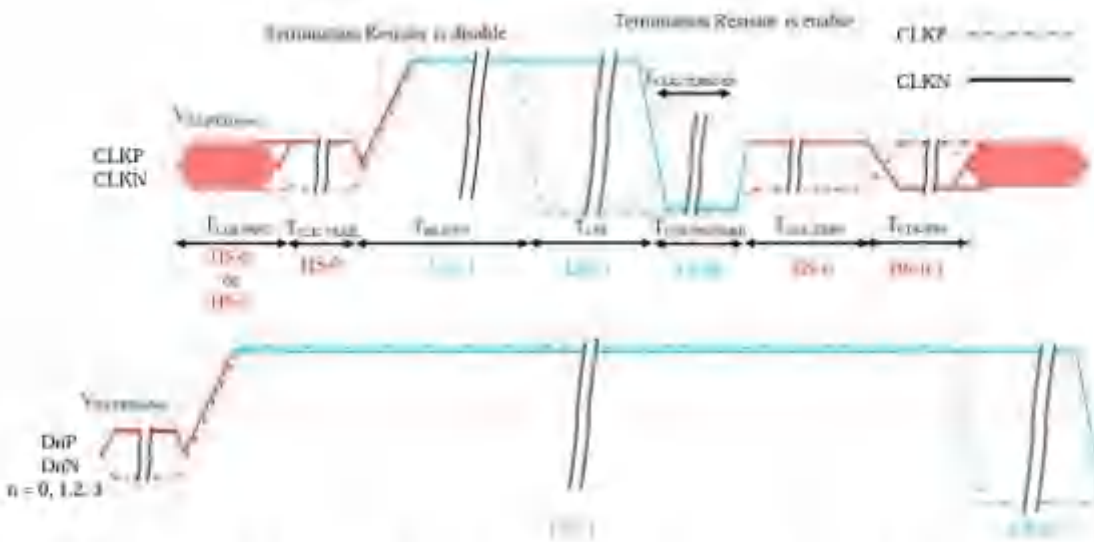
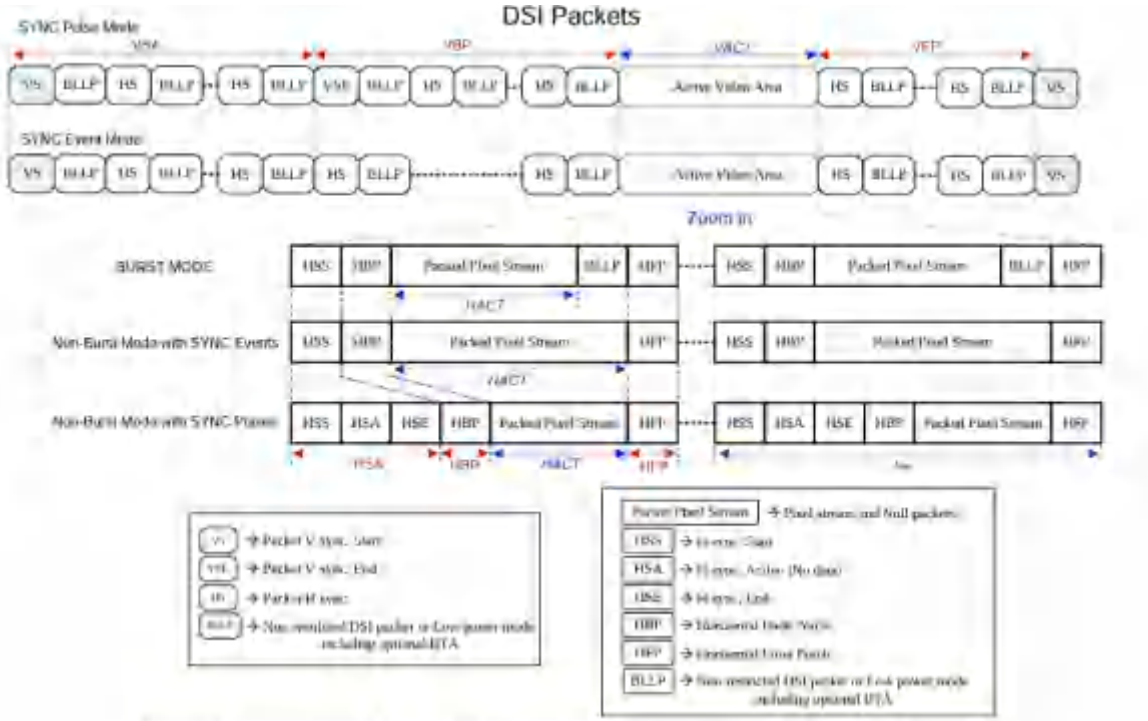


Figure 123: Clock Lanes - High Speed Mode to/from Low Power Mode Timings

Table 46: Clock Lanes - High Speed Mode to/from Low Power Mode Timings

Signal	Symbol	Description	Min	Max	Unit
CLKP/N	$T_{CLK-POST}$	Time that the MCU shall continue sending HS clock after the last associated Data Lanes has transitioned to LP mode	60+52xUI	-	ns
CLKP/N	$T_{CLK-TRAIL}$	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	ns
CLKP/N	$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100	-	ns
CLKP/N	$T_{CLK-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	38	95	ns
CLKP/N	$T_{CLK-TERM-EN}$	Time-out at Clock Lane to enable HS termination	-	38	ns
CLKP/N	$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	Minimum lead HS-0 drive period before starting Clock	300	-	ns
CLKP/N	$T_{CLK-PRE}$	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	8xUI	-	ns

7.3 Timing for DSI video mode



Parameters	Symbols	Min.	Typ.	Max.	Units
Vertical sync. active	VSA	2	-	-	Line
Vertical Back Porch	VBP	14	-	-	Line
Vertical Front Porch	VFP	8	-	-	Line
Active lines per frame	VACT	-	1280	-	Line
Horizontal sync. active	HSA	2	-	-	Pixel
Horizontal Porch period	HSA + HBP + HFP	1.6	-	-	us
Active pixels per line	HACT	-	720	-	Pixel
Bit rate	BR_{bps}	385		Note 5	Mbps/lane

1 UI=1/Bit rate

HSA(pixel) = (tHSA*lane number) / (UI* pixel format)

HBP(pixel) = (tHBP*lane number) / (UI* pixel format)

HFP(pixel) = (tHFP*lane number) / (UI* pixel format)

$$\text{Frame Rate} = \frac{BR_{bps} \times Lane_{num}}{(VACT+VSA+VBP+VFP) \times (HACT+HSA+HBP+HFP) \times \text{Pixel Format}}$$

Example : BR_{bps} = 457Mbps/lane, 1UI=2.1883ns, Frame rate=60Hz, VACT=1280, VSA=2, VBP=30, VFP=20, HACT=720, HSA=33, HBP=100, HFP=100, $Lane_{num}$=4(lane), Pixel Format=24(bit).

Note:

1. $Lane_{num}$: Date lane of MIPI-DSI.

2. Pixel Format: Please reference to“4.1DSI System Interface".

3. The formula exists slightly error because of the host-transmission way.

4. The best frame rate setting:2datalanes :50-60Hz/3 data lanes : 50~70Hz/ 4 data lanes : 50-70 Hz5.Please reference to "Table 39: Limited Clock Channel Speed".

6. The minimum values of this table mean the limitation of IC without considering the panel GIP. The actual values of VSA, VBP and VFP will be changed by different panel GIP setting.

7.4 Reset Timing

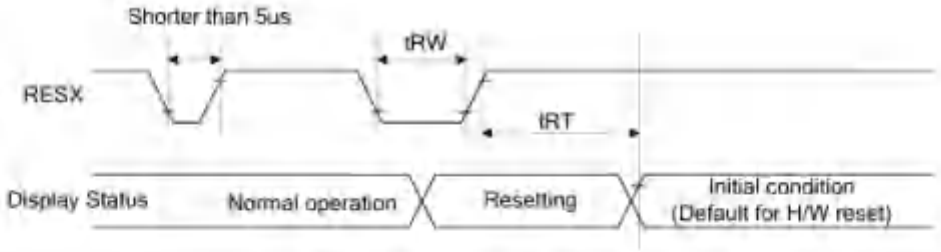


Figure 124: Reset Timing

Table 47: Reset Timing

Signal	Symbol	Parameter	Min	Max	Unit
RESX	tRW	Reset pulse duration	10		uS
	tRT	Reset cancel		5 (note 1,5)	mS
				120 (note 1,6,7)	mS

Notes:

1. *The reset cancel also includes required time for loading ID bytes, VCOM setting and other settings from EEPROM to registers. This loading is done every time when there is H/W reset cancel time (tRT) within 5 ms after a rising edge of RESX.*
2. *Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the Table 48.*

Table 48: Reset Descript

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 10us	Reset
Between 5us and 10us	Reset starts

3. During the Resetting period, the display will be blanked (The display enters the blanking sequence, which maximum time is 120 ms, when Reset Starts in the Sleep Out mode. The display remains the blank state in the Sleep In mode.) and then return to Default condition for Hardware Reset.
4. Spike Rejection can also be applied during a valid reset pulse, as shown below:

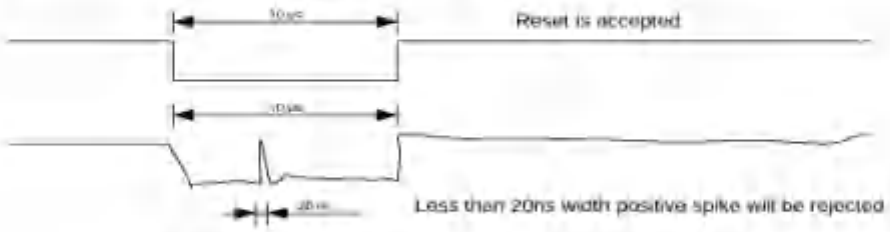
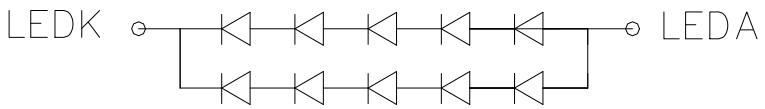


Figure 125: Positive Noise Pulse during Reset Low

5. When Reset applied during Sleep In Mode.
6. When Reset applied during Sleep Out Mode.
7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

8.0 Backlight Characteristic

Backlight LED Circuit:

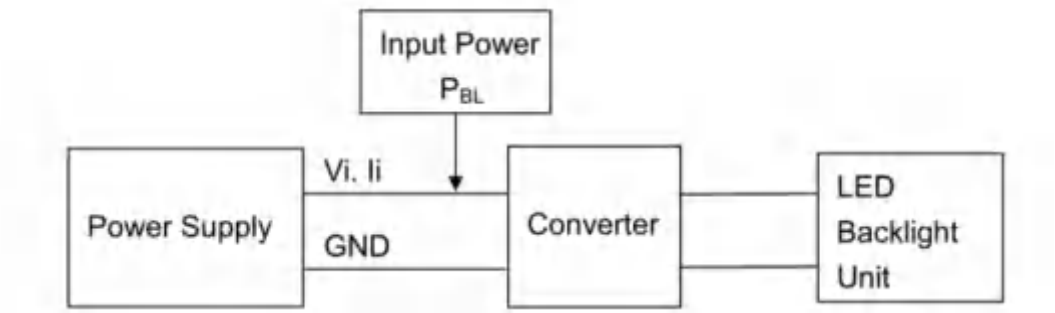


LED BACKLIGHT: Vf=13.5V~16.5V, If=120mA.

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Supply Voltage	Vf	13.5	15	16.5	V	Note 1
Supply Current	If	-	120	-	mA	Note 2
Power dissipation	P_{BL}	-	1.8	-	W	
Life Time	-	30000	-	-	Hr	Note 3,4
Backlight Color	White					

Note 1: The LED Supply Voltage is defined by the number of LED at Ta=25℃ and If =120mA.

Note 2: LED current is measured by utilizing a high frequency current meter as shown below:



Note 3: The “LED life time” is defined as the module brightness decrease to 50% original brightness at Ta=25℃ and If =120mA. The LED lifetime could be decreased if operating If is larger than 120mA.

Note 4: LED light bar circuit:

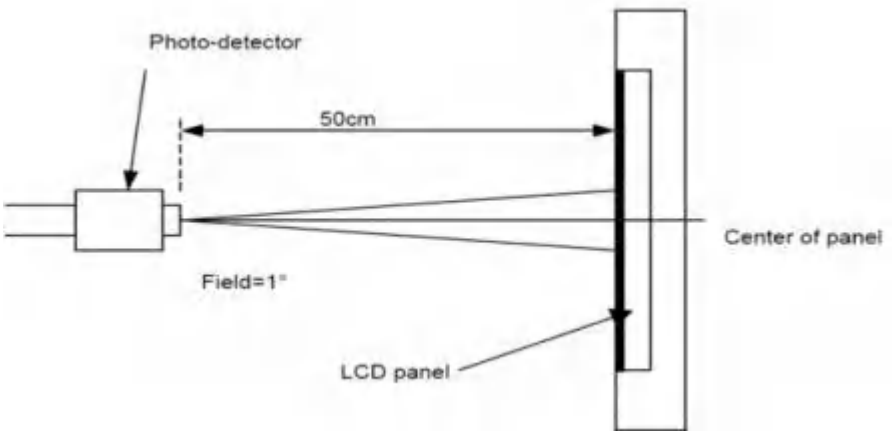
9. Optical Characteristics

Item	Symbol		Condition	Min.	Typ.	Max.	Unit	Note
Brightness	Bp		If=120mA	-	750	-	Cd/m^2	1
Uniformity	⊿Bp			80	-	-	%	1,2
Viewing Angle	3:00		Cr≥10	-	80	-	Deg	1,2
	6:00			-	80	-		
	9:00			-	80	-		
	12:00			-	80	-		
Contrast Ratio	Cr		θ=0° Φ=0°	1000	1200	-	-	3,4
Response Time	T_r+T_f			-	30	35	ms	4,5
Color of CIE Coordinate	W	x	θ=0° Φ=0°	Typ-0.05	TBD	Typ+0.05	-	1,6
		y			TBD		-	
	R	x			TBD		-	
		y			TBD		-	
	G	x			TBD		-	
		y			TBD		-	
	B	x			TBD		-	
		y			TBD		-	
NTSC Ratio	S			-	65	-	%	

*The parameter is slightly changed by temperature, driving voltage and materiel

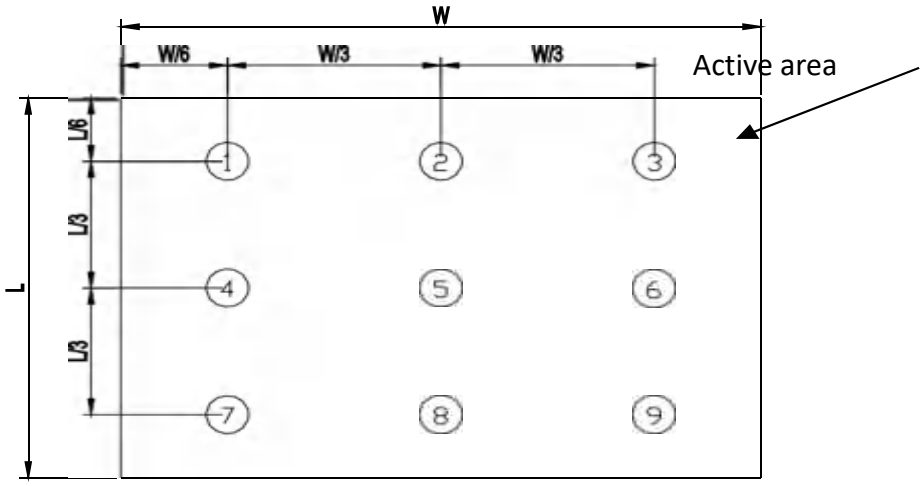
Note 1: The data are measured after LEDs are turned on for 5 minutes. LCM displays full white. The brightness is the average value of 9 measured spots. Measurement equipment CA310 Measuring condition:-Measuring surroundings: Dark room.-Measuring temperature: Ta=25℃.-Adjust operating voltage to get optimum contrast at the center of the display.

The measured value is more than 5 minutes at the center point of the LCD panel, and the backlight is turned on at the same time.

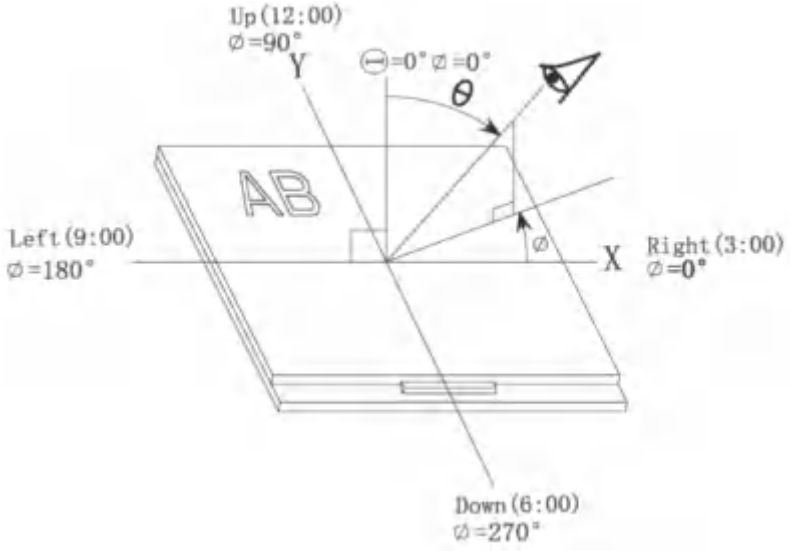


Note 2: The luminance uniformity is calculated by using following formula.

⊿Bp = Bp (Min.) / Bp (Max.)×100 (%);Bp (Max.) = Maximum brightness in 9 measured spots Bp (Min.) = Minimum brightness in 9 measured spots.



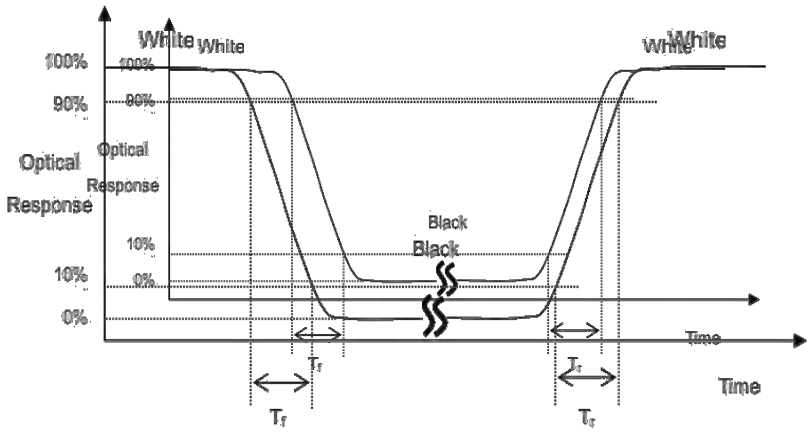
Note 3: The definition of viewing angle:Refer to the graph below marked by θ and Φ



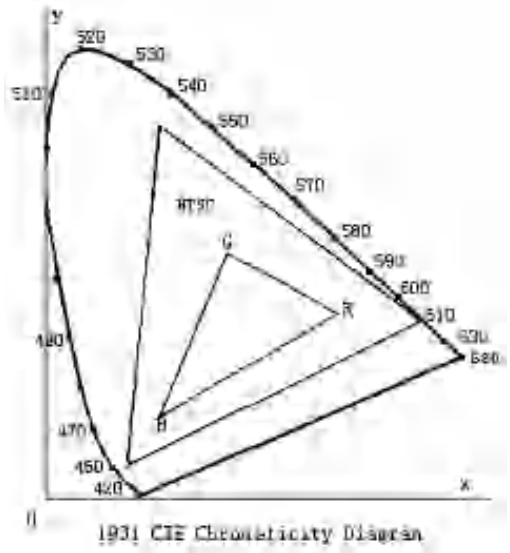
Note 4: Definition of contrast ratio Contrast measurements shall be made at viewing angle of Θ= 0 and at the center of the LCD surface.Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state.

$$\mathbf{CR} = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

Note 5: Definition of Response time The output signals of photo detector are measured when the input signals are changed from “white” to “black”(Tf) and from “black” to “white”(Tr), respectively. The response time is defined as the time interval between the 10% and 90% of amplitudes. Refer to figure as below.



Note 6: Definition of Color of CIE Coordinate and NTSC Ratio.



Color gamut:

$$\mathbf{S} = \frac{\mathbf{area\ of\ RGB\ triangle}}{\mathbf{area\ of\ NTSC\ triangle}} \times \mathbf{100\%}$$

10. Reliability Test Conditions and Methods

No.	Test Items	Test Condition	Inspection After Test
①	High Temperature Storage	80°C±2°C×240Hours	Inspection after 2~4hours storage at room temperature, the samples should be free from defects: 1, Air bubble in the LCD. 2, Seal leak. 3, Non-display. 4, Missing segments. 5, Glass crack. 6, Current IDD is twice higher than initial value. 7, The surface shall be free from damage. 8, The electric characteristic requirements shall be satisfied. 9.Brightness reduction more than 50%.
②	Low Temperature Storage	-30°C±2°C×240Hours	
③	High Temperature Operating	70°C±2°C×240Hours	
④	Low Temperature Operating	-20°C±2°C×240Hours	
⑤	Temperature Cycle(Storage)	-30°C ⟺ 80°C (30min) (5min) (30min) 1cycle Total 10cycle.	
⑥	Damp Proof Test (Storage)	60°C±5°C×90%RH×240Hours	
⑦	Vibration Test	Frequency:10Hz~55Hz~10Hz Amplitude:1.5mm X,Y,Z direction for total 3hours (packing condition test will be tested by a carton).	
⑧	Drooping Test	Drop to the ground from 1M height one time every side of carton. (packing condition test will be tested by a carton).	
⑨	ESD Test	Voltage:±8KV,R:330Ω,C:150PF, Air Mode,5times.	

REMARK:

1, The Test samples should be applied to only one test item.

2, Sample side for each test item is 5~10pcs.

3,For Damp Proof Test, Pure water(Resistance＞10MΩ)should be used.

4,In case of malfunction defect caused by ESD damage, if it would be recovered to normal state after resetting, it would be judge as a good part.

5, EL evaluation should be accepted from reliability test with humidity and temperature: Some defects such as black spot/blemish can happen by natural chemical reaction with humidity and Fluorescence EL has.

6, Failure Judgment Criterion: Basic Specification Electrical Characteristic, Mechanical Characteristic, Optical Characteristic.

11. Inspection Standard

11.1 Scope

Specifications contain
11.1.1 Display Quality Evaluation
11.1.2 Mechanics Specification

11.2 Sampling Plan

Unless there is other agreement, the sampling plan for incoming inspection shall follow MIL-STD-105E.
11.2.1 Lot size: Quantity per shipment as one lot (different model as different lot).
11.2.2 Sampling type: Normal inspection, single sampling.
11.2.3 Sampling level: Level II.
11.2.4 AQL: Acceptable Quality Level
Major defect: AQL=0.65
Minor defect: AQL=1.5

11.3 Panel Inspection Condition

11.3.1 Environment:
Room Temperature: 25±5°C.
Humidity: 65±5% RH.
Illumination: 300 ~ 700 Lux.

11.3.2 Inspection Distance:
35±5 cm

11.3.3 Inspection Angle:
The vision of inspector should be perpendicular to the surface of the Module.
11.3.4 Inspection time：
Perceptibility Test Time: 20 seconds max.

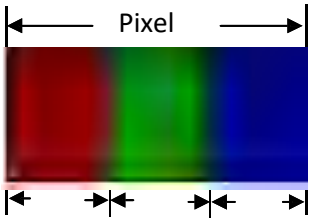
11.4 Inspection Plan

Class	Item	Judgment	Class

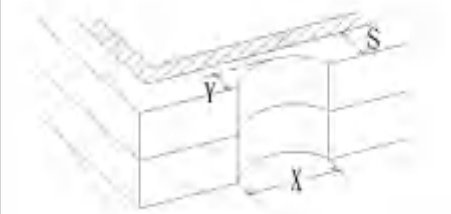
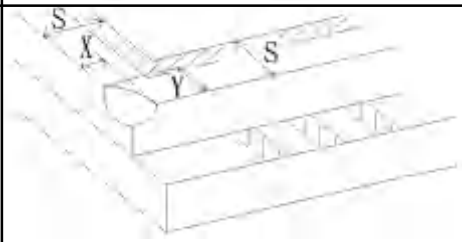
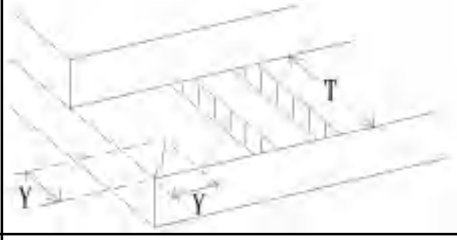
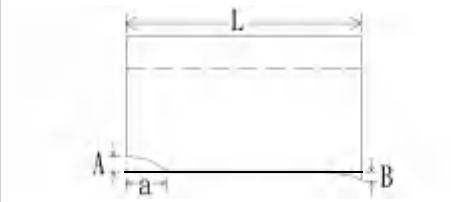
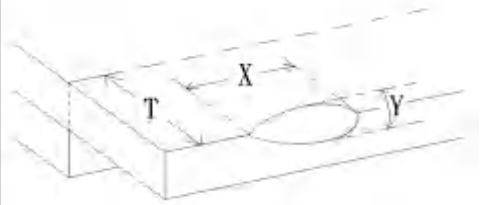
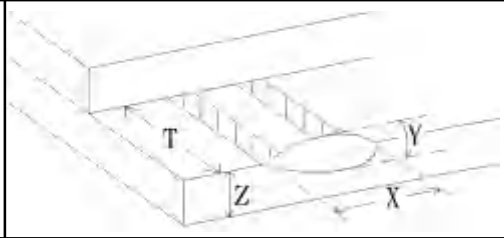
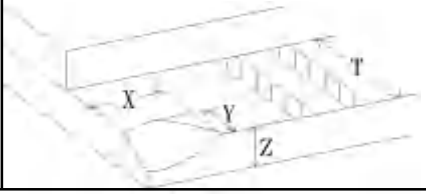
Packing & Indicate	1. Outside and inside package.	"MODEL NO.", "LOT NO." and "QUANTITY" should indicate on the package.	Minor
	2. Model mixed and quantity.	Other model mixed Quantity short or over	Major
	3. Product indication.	"MODEL NO." should indicate on the product.	Major
Assembly	4. Dimension, LCD glass scratch and scribe defect.	According to specification or drawing.	Major
Appearance	5. Viewing area.	Polarizer edge or LCD's sealing line is visible in the viewing area…….Rejected.	Minor
	6. Blemish, black spot, white spot in the LCD and LCD glass cracks.	According to standard of visual inspection.(inside viewing area)	Minor
	7. Blemish, black spot, white spot and scratch on the polarizer.	According to standard of visual inspection.(inside viewing area)	Minor
	8. Bubble in polarizer.	According to standard of visual inspection.(inside viewing area)	Minor
	9. LCD's rainbow color.	Strong deviation color (or newton ring) of LCD……..Rejected. Or according to limited sample.(if needed, and inside viewing area)	Minor
Electrical	10. Electrical and optical characteristics.(contrast Vop chromaticity….etc)	According to specification or drawing.(inside viewing area)	Major
	11. Missing line.	Missing dot line character	Major
	12.Short circuit. Wrong pattern display.	No display, wrong pattern display, current consumption. Out of specification	Major
	13. Dot defect.(for color and TFT)	According to standard of visual Inspection.	Minor

11.5 Standard Of Visual Inspection

NO.	CLASS	ITEM	JUDGMENT

<table>
<tr>
<td>11.5.1</td>
<td>Minor</td>
<td>Black and white spot.
Foreign materiel.
Dust.
Blemish.
Scratch.</td>
<td>(A) Round type: Unit: mm
<table>
<tr><th>Diameter (mm.)</th><th>Acceptable Q'ty</th></tr>
<tr><td>Φ≦0.1</td><td>Disregard</td></tr>
<tr><td>0.1 < Φ≦0.2</td><td>2(Distance>10mm)</td></tr>
<tr><td>0.20 < Φ</td><td>0</td></tr>
</table>
Note: Φ = (length+width)/2
(B) Linear type: Unit: mm
<table>
<tr><th>Length</th><th>Width (mm.)</th><th>Acceptable Q'ty</th></tr>
<tr><td>--</td><td>W≦0.03</td><td>Disregard</td></tr>
<tr><td>L≦3.0</td><td>0.03< W≦0.05</td><td>1(Distance>10mm)</td></tr>
<tr><td>--</td><td>0.05 < W</td><td>Not allow</td></tr>
</table>
</td>
</tr>
<tr>
<td>11.5.2</td>
<td>Minor</td>
<td>Dent on polarizer.</td>
<td>Unit: mm.
<table>
<tr><th>Diameter</th><th>Acceptable Q'ty</th></tr>
<tr><td>Φ≦0.1</td><td>Disregard</td></tr>
<tr><td>0.1 < Φ≦0.2</td><td>2(Distance>10mm)</td></tr>
<tr><td>0.2 < Φ</td><td>0</td></tr>
</table>
</td>
</tr>
<tr>
<td>11.5.3</td>
<td>Minor</td>
<td>Bubble in polarizer.</td>
<td>Unit: mm.
<table>
<tr><th>Diameter</th><th>Acceptable Q'ty</th></tr>
<tr><td>Φ≦0.1</td><td>Disregard</td></tr>
<tr><td>0.1< Φ≦0.25</td><td>2(Distance>10mm)</td></tr>
<tr><td>0.2 < Φ</td><td>0</td></tr>
</table>
</td>
</tr>
<tr>
<td>11.5.4</td>
<td>Minor</td>
<td>Dot defect</td>
<td>
<table>
<tr><th>Items</th><th>Acceptable Q'ty</th></tr>
<tr><td>Bright dot</td><td>N ≦3</td></tr>
<tr><td>Dark dot</td><td>N ≦3</td></tr>
<tr><td>Total dot</td><td>N ≦6</td></tr>
</table>
Pixel define : 

Note1: The definition of dot: The size of a defective dot over 1/2 of whole dot is regarded as one defective dot.
Note 2: Bright dot: Dots appear bright and unchanged in size in which LCD panel is displaying under black pattern.
Note 3: The bright dot defect must be visible through 2% ND filter
Note 4: Dark dot: Dots appear dark and unchanged in size in which LCD panel is displaying under pure red, green, blue
</td>
</tr>
</table>

11.5.5	Minor	LCD glass chipping.		Y>S Reject
11.5.6	Minor	LCD glass chipping.		X or Y>S Reject
11.5.7	Major	LCD glass crack.		Y>(1/2) T Reject
11.5.8	Major	LCD glass scribe defect.		1. a>L/3, A>1.5mm Reject 2. B : According to dimension
11.5.9	Minor	LCD glass chipping. (on the terminal area)		Φ = (x+y)/2>2.5mm Reject
11.5.10	Minor	LCD glass chipping. (on the terminal surface)		Y>(1/3)T Reject
11.5.11	Minor	LCD glass chipping.		Y>T Reject

12. Handling Precautions

12.1 Mounting method

The LCD panel of **APTUS** TFT module consists of two thin glass plates with polarizes which easily be damaged. And since the module in so constructed as to be fixed by utilizing fitting holes in the printed circuit board.

Extreme care should be needed when handling the LCD modules.

12.2 Caution of LCD handling and cleaning

When cleaning the display surface, Use soft cloth with solvent

[Recommended below] and wipe lightly.

- Isopropyl alcohol.
- Ethyl alcohol.

Do not wipe the display surface with dry or hard materials that will damage the polarizer surface.
Do not use the following solvent:

- Water.
- Aromatics.

Do not wipe ITO pad area with the dry or hard materials that will damage the ITO patterns
Do not use the following solvent on the pad or prevent it from being contaminated:

- Soldering flux.
- Chlorine (Cl) , Sulfur (S).

If goods were sent without being silicon coated on the pad, ITO patterns could be damaged due to the corrosion as time goes on.

If ITO corrosion happen by miss-handling or using some materials such as Chlorine (CI), Sulfur (S) from customer, Responsibility is on customer.

12.3 Caution against static charge

The LCD module use C-MOS LSI drivers, so we recommended that you:

Connect any unused input terminal to POWER or GROUND, do not input any signals before power is turned on, and ground your body, work/assembly areas, and assembly equipment to protect against static electricity.

12.4 packing

- Module employs LCD elements and must be treated as such.
- Avoid intense shock and falls from a height.
- To prevent modules from degradation, do not operate or store them exposed direct to sunshine or high temperature/humidity.

12.5 Caution for operation

- It is an indispensable condition to drive LCD's within the specified voltage limit since the higher voltage then the limit cause the shorter LCD life.
- An electro chemical reaction due to direct current causes LCD's undesirable deterioration, so that the use of direct current drive should be avoided.
- Response time will be extremely delayed at lower temperature then the operating temperature range and on the other hand at higher temperature LCD's how dark color in them. However those phenomena do not mean malfunction or out of order with LCD's, which will come back in the specified operation temperature.
- If the display area is pushed hard during operation, some font will be abnormally displayed but it resumes normal condition after turning off once.
- Slight dew depositing on terminals is a cause for electro-chemical reaction resulting in terminal open circuit.

Usage under the maximum operating temperature, 50%Rh or less is required.

12.6 storing

In the case of storing for a long period of time for instance, for years for the purpose or replacement use, the following ways are recommended.

- Storage in a polyethylene bag with the opening sealed so as not to enter fresh air outside in it. And with no desiccant.
- Placing in a dark place where neither exposure to direct sunlight nor light's keeping the storage temperature range.
- Storing with no touch on polarizer surface by the anything else.

[It is recommended to store them as they have been contained in the inner container at the time of delivery from us.

12.7 Safety

- It is recommendable to crash damaged or unnecessary LCD's into pieces and wash off liquid crystal by either of solvents such as acetone and ethanol, which should be burned up later.
- When any liquid leaked out of a damaged glass cell comes in contact with your hands, please wash it off well with soap and water.

13. Precaution for Use

13.1

A limit sample should be provided by the both parties on an occasion when the both parties agreed its necessity. Judgment by a limit sample shall take effect after the limit sample has been established and confirmed by the both parties.

13.2

On the following occasions, the handing of problem should be decided through discussion and agreement between responsible of the both parties.

- When a question is arisen in this specification
- When a new problem is arisen which is not specified in this specifications
- When an inspection specifications change or operating condition change in customer is reported to **APTUS** TFT , and some problem is arisen in this specification due to the change
- When a new problem is arisen at the customer's operating set for sample evaluation in the customer site.