SHENZHEN APTUS TECHNOLOGY CO., LIMITED

PRODUCT SPECIFICATION

22" 2560*1024 LCD MODULE

MODEL NAME: DBC220AZN40-30L100A

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FOR CUSTOMER	
CUSTOMER APPROVED	

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Record of Revision

Version	Date	Page	Old description	New Description	Remark
1.0	2024/9/04	All	First Version release		

1 Handling Precautions

1) Since polarizer is easily damaged, do not touch or press the surface of polorizer with hand.
2) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
3) When the cell surface is soiled, wipe it with absorbent cotton or other soft cloth.
4) Since the cell is made of glass, it may break or crack if dropped or bumped on hard surface.
5) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
6) Do not press or pat the panel surface by fingers, hand or tooling.
7) Please handle TFT cell with care. The FPCs can only sustain for quite limited stress.
8) The cell package tray is packed in clean room. Please do pack & unpack it in clean room.
9) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT cell.
10) Pls avoid touching COF position while you are doing mechanical design.
11) When storing modules as spares for a long time, the following precaution is necessary:
    Store them in a dark place. Do not expose the module to sunlight or fluorescent light. Keep the temperature between 5℃and 35℃ at normal humidity.
12) Do not apply the same pattern for a long time, it will enhance relevant defect.

2 General Description

This specification applies to the 22 inch wide Color a-Si TFT-LCD Module DBC220AZN40-30L100A. The display supports the QHD - 2560(H) x 1024(V) screen format and 16.7M colors (RGB 6-bits + Hi-FRC data). The input interface is 4 channel LVDS

2.1 Display Characteristics

The following items are characteristics summary on the table under 25℃ condition:

ITEMS	Unit	SPECIFICATIONS	
Screen Diagonal	[inch]	22”	
Active Area	[mm]	526.85(H)mm x 210.74(V)mm	
Outline Dimension	[mm]	550.00×236.00×14.00	
Pixels H x V	-	2560(x3)x1024	
Pixel Pitch	[um]	205.8(H)um x 205.8(V)um	
Pixel Arrangement	-	R.G.B. Vertical Stripe	
Display Mode	-	AHVA, normally Black	
Response Time	[msec]	14 (Typ., on/off)	
Power Consumption	[Watt]	9.0 (Typ.) @ White pattern,Fv=60Hz	
Weight	[Grams]	T.B.D (Typ)	
Electrical Interface	-	4 channel LVDS, 8 bits RGB data input	
Support Color	-	16.7M colors (RGB 6-bit + Hi_FRC)	
Surface Treatment	-	Anti-Glare, 3H	
Temperature Range Operating Storage (Shipping)	[ºC]	 0 to +50 -20 to +60	
Cell transmittance	[%]	3.3 (typ.) 3 (min)	Base on AUO LED Backlight

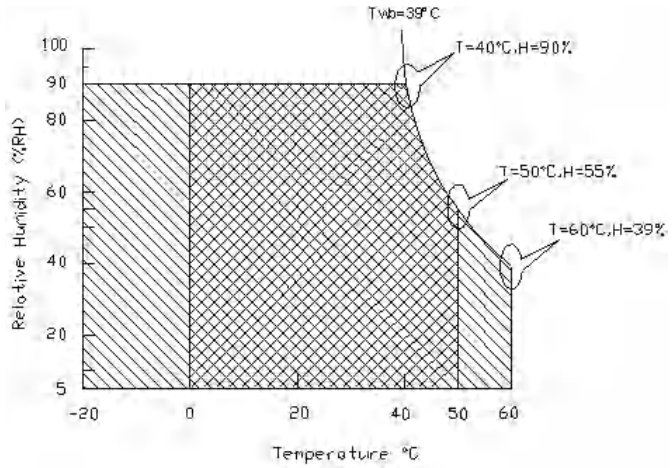
2.2 Absolute Maximum Rating of Environment

Permanent damage may occur if exceeding the following maximum rating.

Symbol	Description	Min.	Max.	Unit	Remark
TOP	Operating Temperature	0	+50	[°C]	***Note 2-1***
TGS	Glass surface temperature (operation)	0	+65	[°C]	***Note 2-1*** *Function judged only*
HOP	Operation Humidity	5	90	[%RH]	***Note 2-1***
TST	Storage Temperature	-20	+60	[°C]	
HST	Storage Humidity	5	90	[%RH]	

Note 2-1: Temperature and relative humidity range are shown as the below figure.

1. 90% RH Max (Ta≦39℃)
2. Max wet-bulb temperature at 39℃ or less. (Ta≦39℃)
3. No condensation



Operating Range Storage Range +

2.3 Optical Characteristics

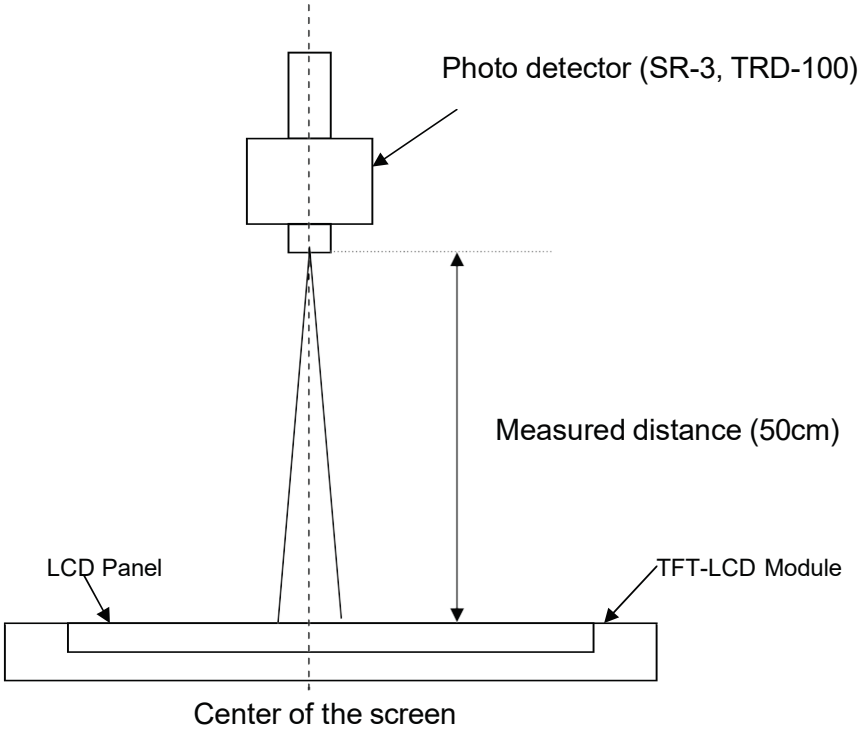
The optical characteristics are measured on the following test condition.

Test Condition:

1. Equipment setup: Please refer to *Note 2-2*.
2. Panel Lighting time: 30 minutes
3. VDD=5.0V, Fv=60Hz, Ta=25℃

Symbol	Description		Min	Typ.	Max	Unit	Remark
CR	Contrast Ratio (Center of screen)		600	1000	-	-	Note 2-3 Base on AUO LED Backlight
θ_R	Horizontal Viewing Angle (CR=10)	Right	75	89	-	[degree]	*Note 2-4* *By SR-3*
θ_L		Left	75	89	-		
Φ_H	Vertical Viewing Angle (CR=10)	Up	75	89	-		
Φ_L		Down	75	89	-		
θ_R	Horizontal Viewing Angle (CR=5)	Right	75	89	-		
θ_L		Left	75	89	-		
Φ_H	Vertical Viewing Angle (CR=5)	Up	75	89	-		
Φ_L		Down	75	89	-		
T_{GTG}	Response Time	Gray to Gray	-	14	-	[msec]	*Note 2-5* *By TRD-100*
R_x	Color Coordinates (CIE 1931)	Red x	0.632	0.662	0.692		Base on C light
R_y		Red y	0.294	0.324	0.354		
G_x		Green x	0.231	0.261	0.291		
G_y		Green y	0.570	0.600	0.630		
B_x		Blue x	0.106	0.136	0.166		
B_y		Blue y	0.061	0.091	0.121		
W_x		White x	0.288	0.318	0.348		
W_y		White y	0.337	0.367	0.397		
CT	Crosstalk		-	-	1.5	[%]	*Note 2-6* *By SR-3*
F_{dB}	Flicker (Center of screen)		-	-	-20	[dB]	*Note 2-7* *By SR-3*

Note 2-2: Equipment setup :



Note 2-3: Contrast Ratio Measurement

Definition:

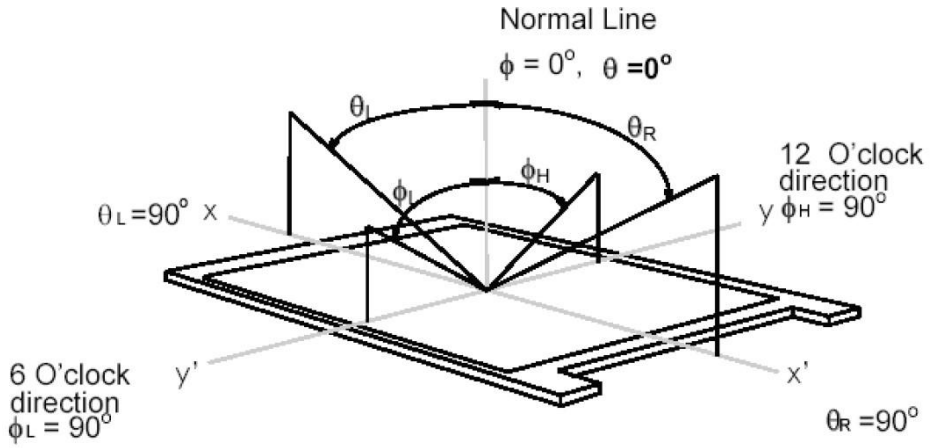
$$\text{Contrast Ratio} = \frac{\text{Luminance of White pattern}}{\text{Luminance of Black pattern}}$$

a. Measured position: Center of screen (P5) & perpendicular to the screen (θ=Φ=0°)

Note 2-4: Viewing angle measurement

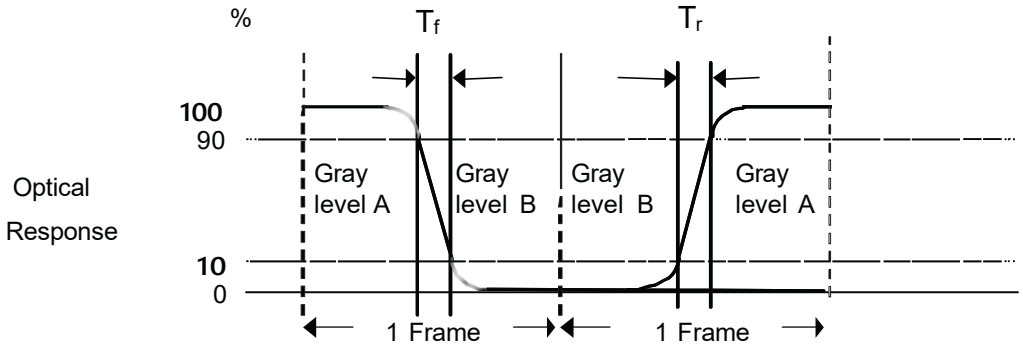
Definition: The angle at which the contrast ratio is greater than 10 & 5 .

a. Horizontal view angle: Divide to left & right (θ_L & θ_R)
Vertical view angle: Divide to up & down (Φ_H &Φ_L)
Vertical view angle: Divide to up & down (Φ_H &Φ_L)



Note 2-5: Response time measurement

The output signals of photo detector are measured when the input signals are changed from “Gray level A” to “Gray level B” (falling time, TF), and from “Gray level B” to “Gray level A” (rising time, TR), respectively. The response time is interval between the 10% and 90% of optical response.



The gray to gray response time is defined as the following table.

Gray Level to Gray Level		Target gray level				
		L0	L63	L127	L191	L255
Start gray level	L0					
	L63					
	L127					
	L191					
	L255					

- T_{GTG_typ} is the total average time at rising time and falling time of gray to gray.

Note 2-6: Crosstalk measurement

Definition:

$CT = Max. (CT_H, CT_V)$;

Where

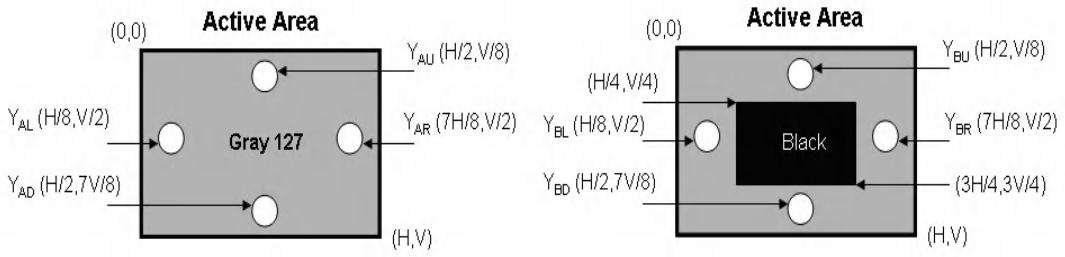
a. Maximum Horizontal Crosstalk :

$CT_H = Max. (| Y_{BL} – Y_{AL} | / Y_{AL} \times 100\ \%, | Y_{BR} – Y_{AR} | / Y_{AR} \times 100\ \%)$;

Maximum Vertical Crosstalk:

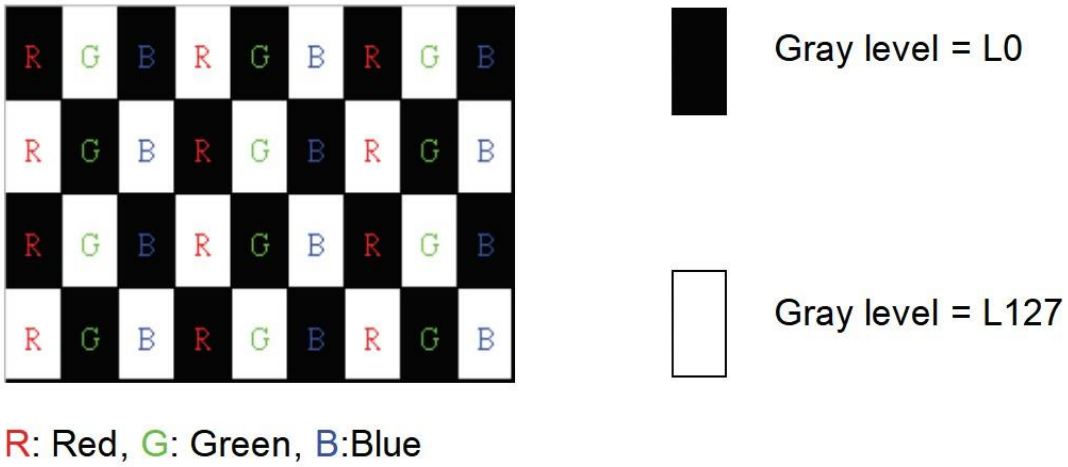
$CT_V = Max. (| Y_{BU} – Y_{AU} | / Y_{AU} \times 100\ \%, | Y_{BD} – Y_{AD} | / Y_{AD} \times 100\ \%)$;

b. Y_{AU}, Y_{AD}, Y_{AL}, Y_{AR} = Luminance of measured location without Black pattern Y_{BU}, Y_{BD}, Y_{BL}, Y_{BR} = Luminance of measured location with Black pattern



Note 2-7: Flicker measurement

a. Test pattern: It is listed as following.

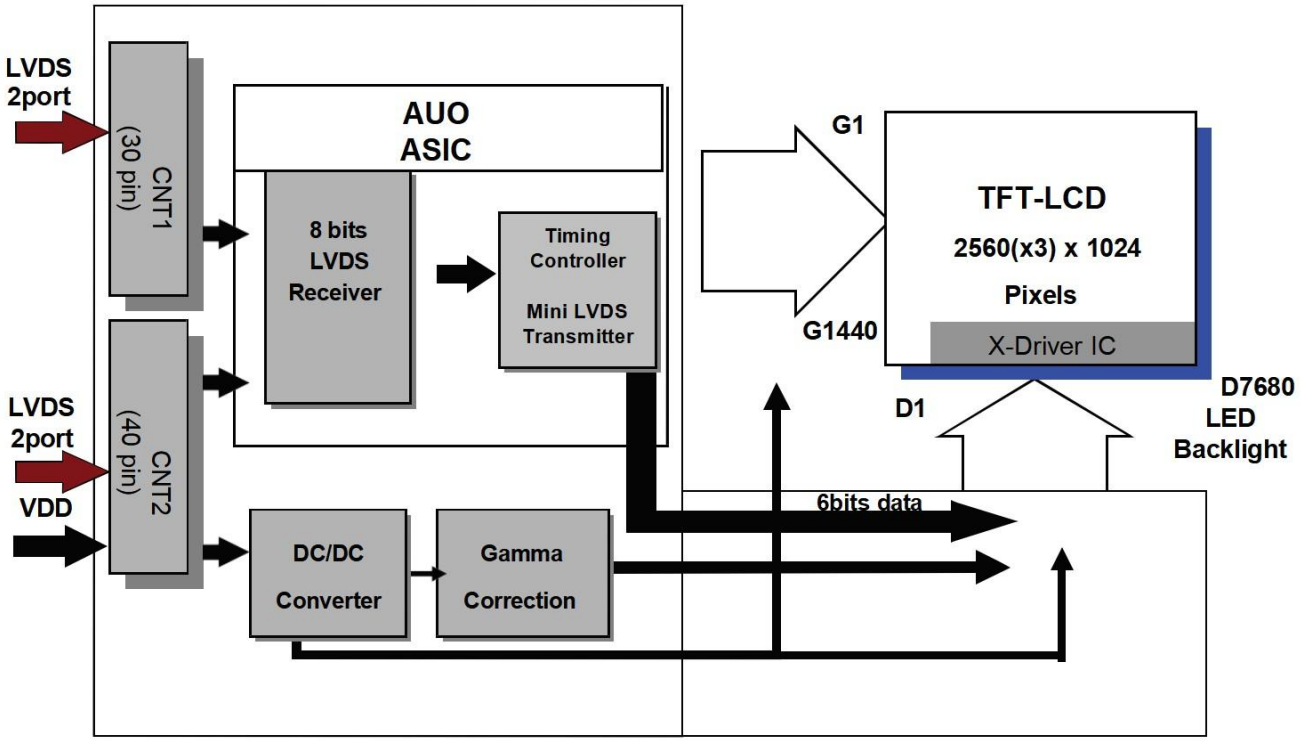


b. Measured position: Center of screen & perpendicular to the screen

3 TFT-LCD Module

3.1 Block Diagram

The following shows the block diagram of the 22 inch Color TFT-LCD Module.



3.2 Interface Connection

3.2.1 Connector Type

TFT-LCD Connector (CNT1)	Manufacturer	STM	P-TWO
	Part Number	MSBKT2407P30HB	187034-3009
TFT-LCD Connector (CNT2)	Manufacturer	Starconn	Fullconn
	Part Number	115F40-S000RA-M3	WF01-415-4032
Mating Connector (CNT1)	Manufacturer	STM or Compatible	
	Part Number	PK2407P30V or Compatible	
Mating Connector (CNT2)	Manufacturer	JAE or Compatible	
	Part Number	FI-NX40HL or Compatible	

3.2.2 Connector Pin Assignment

LVDS CN1

PIN #	Symbol	Description	Remark
1	CH1_0-	FIRST_ Negative LVDS differential data input	
2	CH1_0+	FIRST_ Positive LVDS differential data input	
3	CH1_1-	FIRST_ Negative LVDS differential data input	
4	CH1_1+	FIRST_ Positive LVDS differential data input	
5	CH1_2-	FIRST_ Negative LVDS differential data input	
6	CH1_2+	FIRST_ Positive LVDS differential data input	
7	GND	Power Ground	
8	CH1_CLK-	FIRST_ Negative LVDS differential clock input	
9	CH1_CLK+	FIRST_ Positive LVDS differential clock input	
10	GND	Power Ground	
11	CH1_3-	FIRST_ Negative LVDS differential data input	
12	CH1_3+	FIRST_ Positive LVDS differential data input	
13	NC	No Connection (for AUO test only. Do not connect)	
14	NC	No Connection (for AUO test only. Do not connect)	
15	GND	Power Ground	
16	CH2_0-	SECOND_ Negative LVDS differential data input	
17	CH2_0+	SECOND_ Positive LVDS differential data input	
18	CH2_1-	SECOND_ Negative LVDS differential data input	
19	CH2_1+	SECOND_ Positive LVDS differential data input	

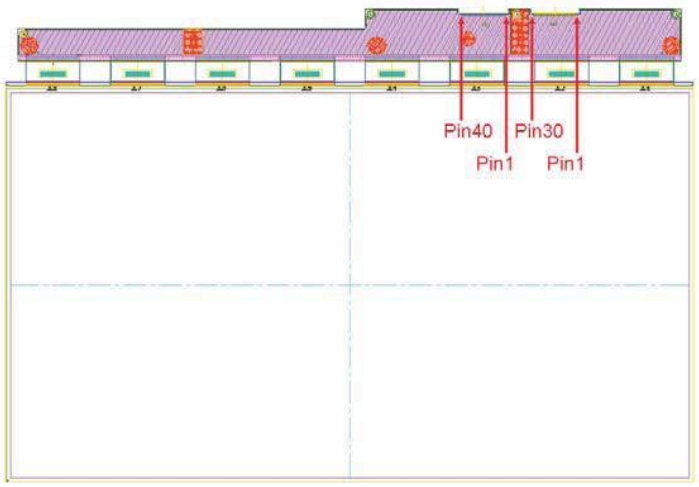
20	CH2_2-	SECOND_ Negative LVDS differential data input	
21	CH2_2+	SECOND_ Positive LVDS differential data input	
22	GND	Power Ground	
23	CH2_CLK-	SECOND_ Negative LVDS differential clock input	
24	CH2_CLK+	SECOND_ Positive LVDS differential clock input	
25	GND	Power Ground	
26	CH2_3-	SECOND_ Negative LVDS differential data input	
27	CH2_3+	SECOND_ Positive LVDS differential data input	
28	NC	No Connection (for AUO test only. Do not connect)	
29	NC	No Connection (for AUO test only. Do not connect)	
30	NC	No Connection (for AUO test only. Do not connect)	

LVDS CN2

PIN #	Symbol	Description	Remark
1	CH3_0-	THIRD_ Negative LVDS differential data input	
2	CH3_0+	THIRD_ Positive LVDS differential data input	
3	CH3_1-	THIRD_ Negative LVDS differential data input	
4	CH3_1+	THIRD_ Positive LVDS differential data input	
5	CH3_2-	THIRD_ Negative LVDS differential data input	
6	CH3_2+	THIRD_ Positive LVDS differential data input	
7	GND	Power Ground	
8	CH3_CLK-	THIRD_ Negative LVDS differential clock input	
9	CH3_CLK+	THIRD_ Positive LVDS differential clock input	
10	GND	Power Ground	
11	CH3_3-	THIRD_ Negative LVDS differential data input	
12	CH3_3+	THIRD_ Positive LVDS differential data input	
13	NC	No Connection (for AUO test only. Do not connect)	
14	NC	No Connection (for AUO test only. Do not connect)	
15	GND	Power Ground	
16	CH4_0-	FOURTH_ Negative LVDS differential data input	
17	CH4_0+	FOURTH_ Positive LVDS differential data input	
18	CH4_1-	FOURTH_ Negative LVDS differential data input	
19	CH4_1+	FOURTH_ Positive LVDS differential data input	
20	CH4_2-	FOURTH_ Negative LVDS differential data input	
21	CH4_2+	FOURTH_ Positive LVDS differential data input	

22	GND	Power Ground	
23	CH4_CLK-	FOURTH_ Negative LVDS differential clock input	
24	CH4_CLK+	FOURTH_ Positive LVDS differential clock input	
25	GND	Power Ground	
26	CH4_3-	FOURTH_ Negative LVDS differential data input	
27	CH4_3+	FOURTH_ Positive LVDS differential data input	
28	NC	No Connection (for AUO test only. Do not connect)	
29	NC	No Connection (for AUO test only. Do not connect)	
30	NC	No Connection (for AUO test only. Do not connect)	
31	NC	No Connection (for AUO test only. Do not connect)	
32	NC	No Connection (for AUO test only. Do not connect)	
33	IMS	Interlace Mode Selection	Note1
34	NC	No Connection (for AUO test only. Do not connect)	
35	GND	Power Ground	
36	VDD	Power +5V	
37	VDD	Power +5V	
38	VDD	Power +5V	
39	VDD	Power +5V	
40	VDD	Power +5V	

Note 1: IMS is Interlace mode selection pin. (Low: Normal Mode, High: Interlace mode. Low level Input Voltage: 0V~0.5V, High level Input Voltage: 2.97 ~ 3.63V, Absolute maximum ratings: -0.5 ~ 4V). If users don't use this function, it should be connected to GND.



3.3 Electrical Characteristics

3.3.1 Absolute Maximum Rating

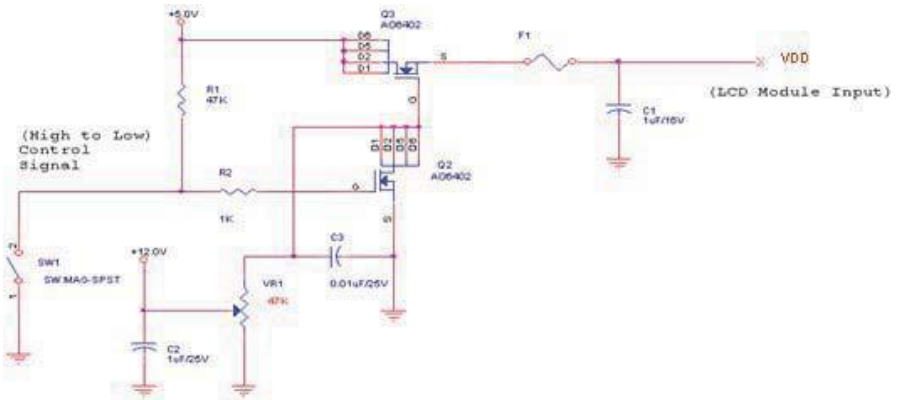
Permanent damage may occur if exceeding the following maximum rating.

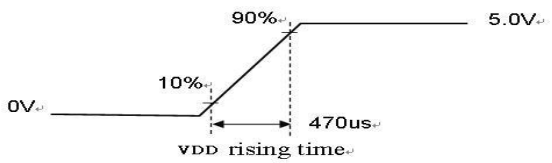
Symbol	Description	Min	Max	Unit	Remark
VDD	Power Supply Input Voltage	GND-0.3	6.0	[Volt]	Ta=25℃

3.3.2 Recommended Operating Condition

Symbol	Description	Min	Typ	Max	Unit	Remark
VDD	Power supply Input voltage	4.5	5.0	5.5	[Volt]	
IDD	Power supply Input Current (RMS)	-	1.8	2.2	[A]	VDD= 5.0V, White Pattern, Fv=60Hz
		-	2.1	2.6	[A]	VDD= 5.0V, White Pattern, Fv=75Hz
PDD	VDD Power Consumption	-	9	11	[Watt]	VDD= 5.0V, White Pattern, Fv=60Hz
		-	10.5	13	[Watt]	VDD= 5.0V, White Pattern, Fv=75Hz
IRush	Inrush Current	-	-	3.0	[A]	*Note 3-1*
VDDrp	Allowable VDD Ripple Voltage	-	-	500	[mV]	VDD= 5.0V, White Pattern, Fv=75Hz

Note 3-1: Inrush Current measurement: Test circuit:

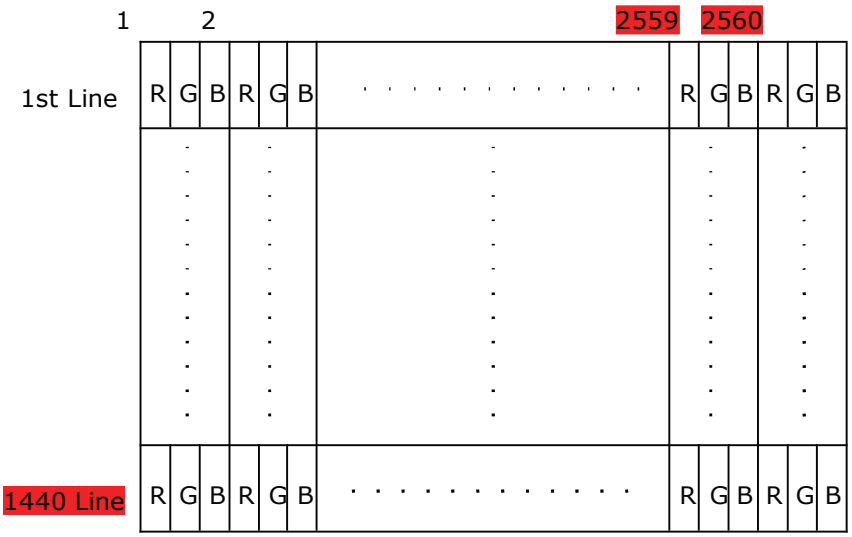




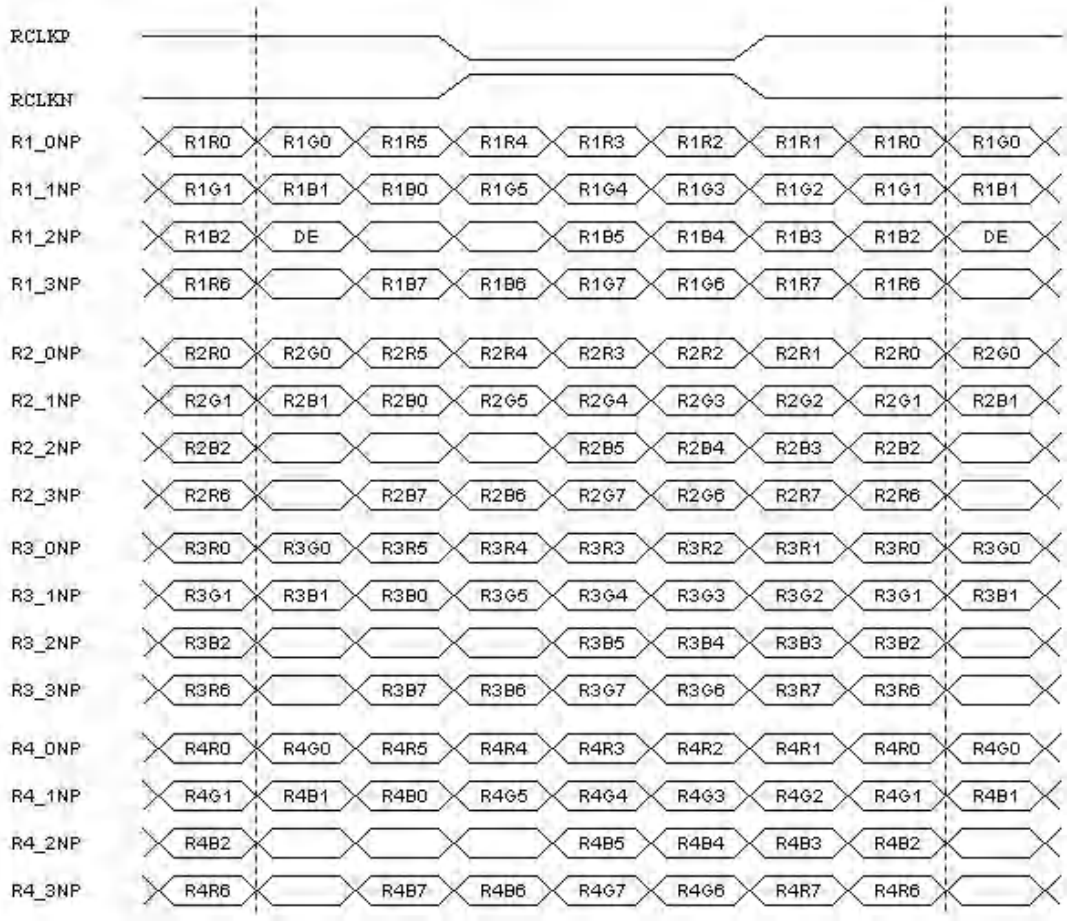
The duration of VDD rising time: 470us.

3.4 Signal Characteristics

3.4.1 LCD Pixel Format



3.4.2 LVDS Data Format



Note 3-2: LVDS Data Mapping of NS Format for Quad Channel

3.4.3 Color versus Input Data

The following table is for color versus input data (8bit). The higher the gray level, the brighter the color.

Color	Gray Level	Color Input Data																								Remark
		RED data (MSB:R7, LSB:R0)								GREEN data (MSB:G7, LSB:G0)								BLUE data (MSB:B7, LSB:B0)								
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0	
Black	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
White	-	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
Gray 127	-	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	
Red	L0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Black
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	L255	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
Green	L0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Black
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	L255	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	
Blue	L0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Black
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	L255	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	

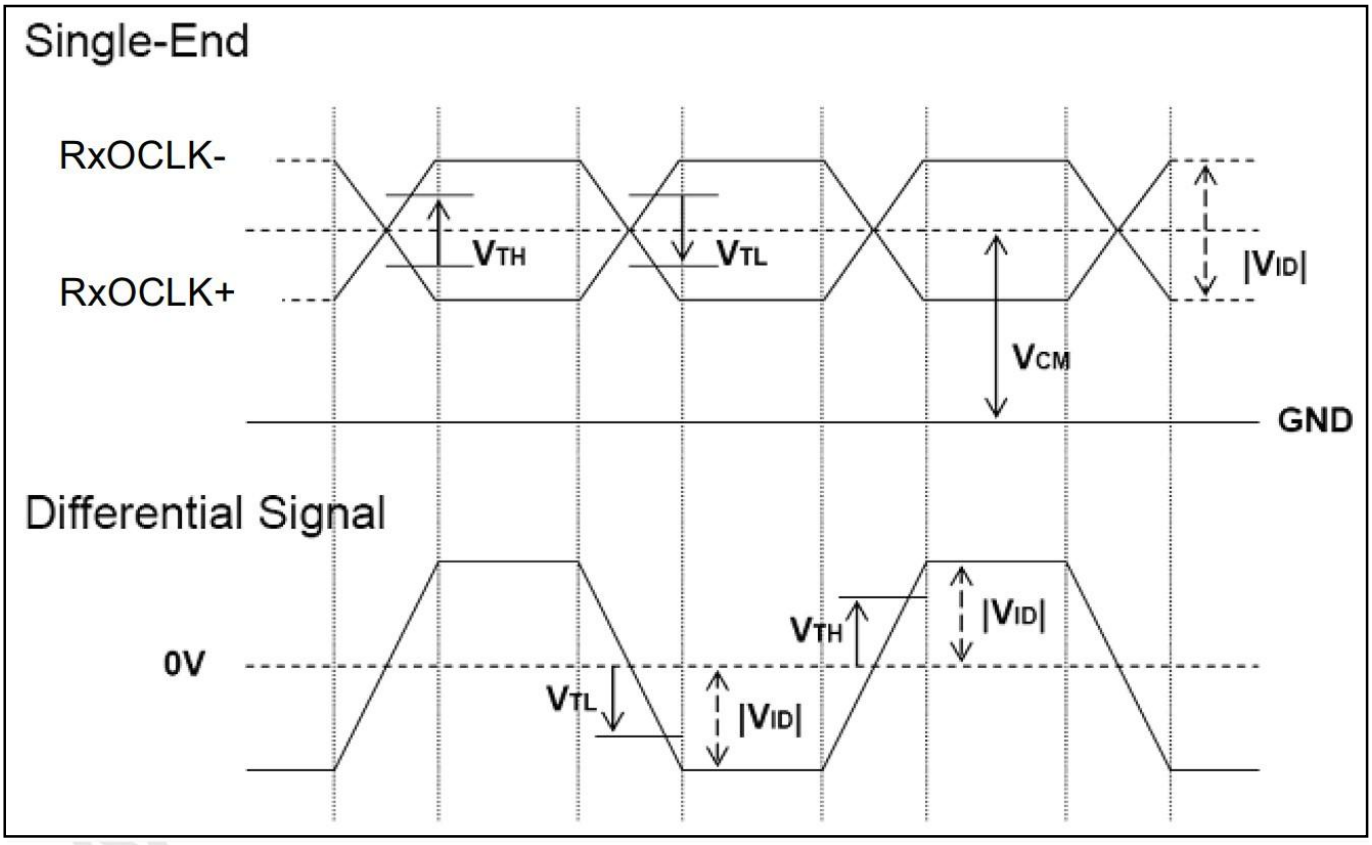
3.4.4 LVDS Specification

a. DC Characteristics:

Symbol	Description	Min	Typ	Max	Units	Condition
V_{TH}	LVDS Differential Input High Threshold	-	-	+100	[mV]	V_{CM} = 1.2V
V_{TL}	LVDS Differential Input Low Threshold	-100	-	-	[mV]	V_{CM} = 1.2V
$\lvert V_{ID} \rvert$	LVDS Differential Input Voltage	100	-	600	[mV]	
V_{CM}	LVDS Common Mode Voltage	+1.0	+1.2	+1.5	[V]	V_{TH}-V_{TL} = 200mV

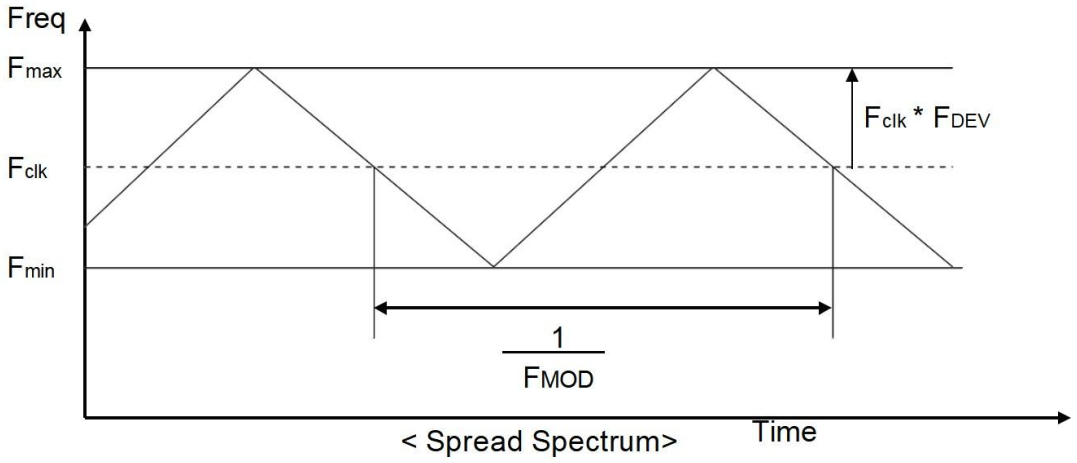
LVDS Signal Waveform:

Use RxOCLK- & RxOCLK+ as example.



b. AC Characteristics:

Symbol	Description	Min	Max	Unit	Remark
F_{DEV}	Maximum deviation of input clock frequency during Spread Spectrum	-	± 3	%	
F_{MOD}	Maximum modulation frequency of input clock during Spread Spectrum	-	200	KHz	



Fclk: LVDS Clock Frequency

3.4.5 Input Timing Specification

It only support DE mode, and the input timing are shown as the following table.

Symbol	Description		Min.	Typ.	Max.	Unit	Remark
Tv	Vertical Section	Period	1452	1481	2347	Th	
Tdisp (v)		Active	1440	1440	1440	Th	
Tblk (v)		Blanking	12	41	907	Th	
Fv		Frequency	49	60	76	Hz	
Th	Horizontal Section	Period	679	680	1023	Tclk	
Tdisp (h)		Active	640	640	640	Tclk	
Tblk (h)		Blanking	39	40	383	Tclk	
Fh		Frequency	71.1	88.8	112	KHz	*Note 3-3*
Tclk	LVDS Clock	Period	13.1	16.6	20.7	ns	1/Fclk
Fclk		Frequency	48.3	60.4	76.5	MHz	*Note 3-4*

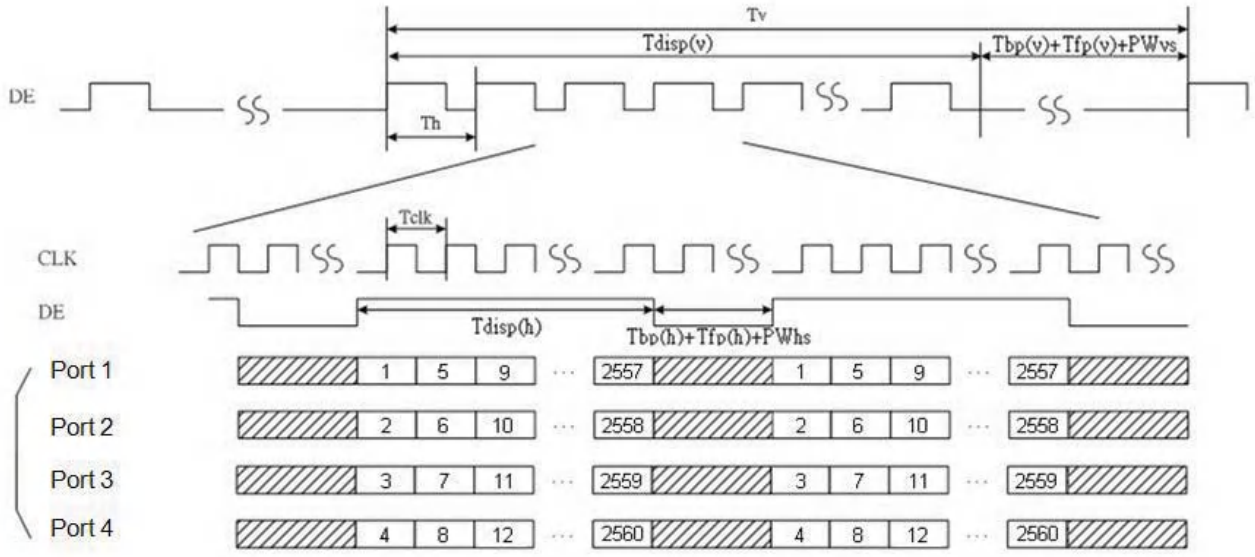
Note 3-3: The equation is listed as following. Please don't exceed the above recommended value.

Fh (Min.) = Fclk (Min.) / Th (Min.);
Fh (Typ.) = Fclk (Typ.) / Th (Typ.);
Fh (Max.)= Fclk (Max.) / Th (Min.);

Note 3-4: The equation is listed as following. Please don't exceed the above recommended value.

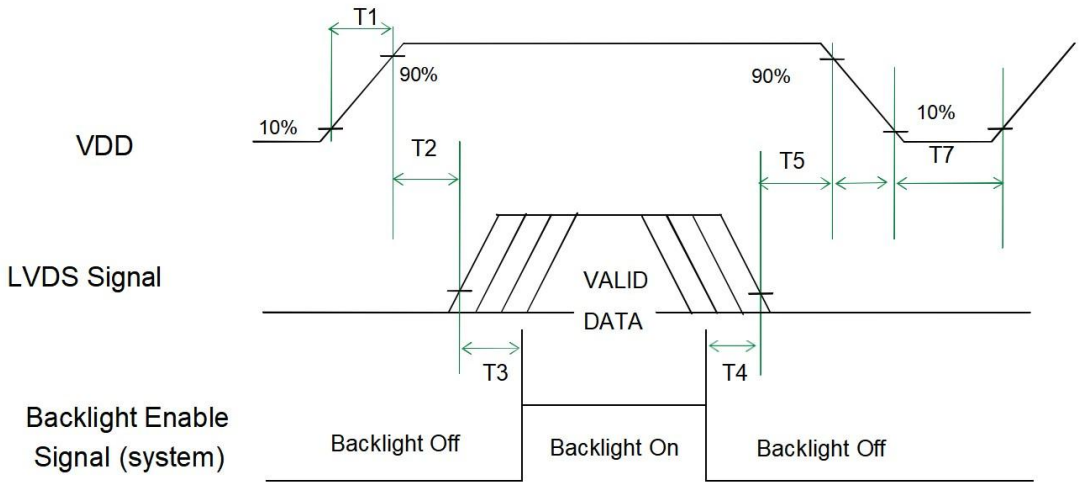
Fclk (Min.) = Fv (Min.) x Th (Min.) x Tv (Min.);
Fclk (Typ.) = Fv (Typ.) x Th (Typ.) x Tv (Typ.);
Fclk (Max.) = Fv (Max.) x Th (Typ.) x Tv (Typ.);

3.4.6 Input Timing Diagram



3.5 Power ON/OFF Sequence

VDD power,LVDS signal and backlight on/off sequence are as following. LVDS signals from any system shall be Hi-Z state when VDD is off.



Power Sequence Timing

Symbol	Value			Unit	Remark
	Min.	Typ.	Max.		
T1	0.5	-	10	[ms]	
T2	0	-	50	[ms]	
T3	500	-	-	[ms]	
T4	100	-	-	[ms]	
T5	0		50	[ms]	*Note 3-5*
T6	0	-	200	[ms]	*Note 3-6* *Note 3-7*
T7	1000	-	-	[ms]	

Note 3-5 : Recommend setting T5 = 0ms to avoid electronic noise when VDD is off.
Note 3-6 : During T5 period , please keep the level of input LVDS signals with Hi-Z state.

4 Reliability Test

Reliability test items are listed as following table. (*Bare Panel only*)

Items	Condition	Remark
Temperature Humidity Bias (THB)	Ta= 50℃, 80%RH, 300hours	
High Temperature Operation (HTO)	Ta= 50℃, 50%RH, 300hours	
Low Temperature Operation (LTO)	Ta= 0℃, 300hours	
High Temperature Storage (HTS)	Ta=60℃, 300hours	
Low Temperature Storage (LTS)	Ta=-20℃, 300hours	
Thermal Shock Test (TST)	-20℃/30min, 60ɗ/30min, 100 cycles	*Note 4-1*

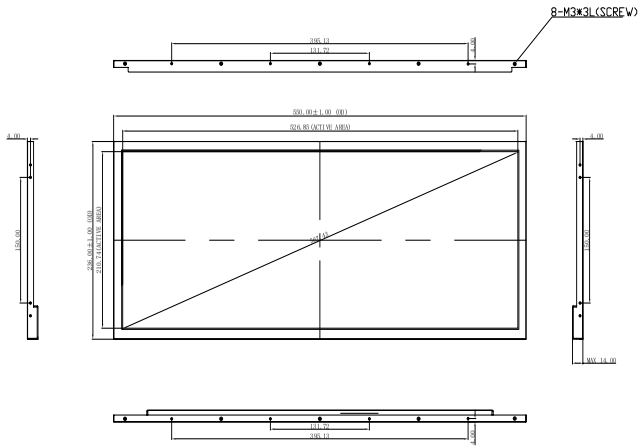
Note 4-1: a. A cycle of rapid temperature change consists of varying the temperature from -20℃to 60℃, and back again. Power is not applied during the test.

b. After finish temperature cycling, the unit is placed in normal room ambient for at least 4 hours before power on.

6 Mechanical Characteristic

TECHNOLOGY CHARACTERISTICS LCM	
SIZE	22inch
Resolution ratio	2560*1024
Display mode	Transmissive Normally Black
Display direction	□ 6 □ 12 □ 3 □ 9 ■ Free
Contrast ratio	1000:1
Luminance	1000 typ
Uniformity	80% MIN
Interface	LVDS
Power supply	■ 5.0 □ 3.3
Operation temperature	0~50
Storage temperature	-20~60

标记	内容	日期	签名

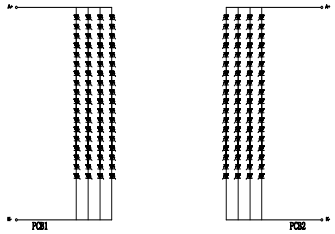


灯条接口：

CN2/3:PH2.0-2PIN（2路）	
NO.	Definition
1	V+
2	V-

灯条参数：

1.线路图：



LED CIRCUIT 18*4=72EA, 90mA*4=360mA

2. LED规格 4014LED (120mA/LED)
电压：50.4-59.4V 电流：360mA*2

屏线接口：

CN1:			
NO.	Definition		
1	CH1_0-	21	CH2_2+
2	CH1_0+	22	GND
3	CH1_1-	23	CH2_CLK-
4	CH1_1+	24	CH2_CLK+
5	CH1_2-	25	GND
6	CH1_2+	26	CH2_3-
7	GND	27	CH2_3+
8	CH1_CLK-	28	NC
9	CH1_CLK+	29	NC
10	GND	30	NC
11	CH1_3-		
12	CH1_3+		
13	NC		
14	NC		
15	GND		
16	CH2_0-		
17	CH2_0+		
18	CH2_1-		
19	CH2_1+		
20	CH2_2-		

CN2:			
NO.	Definition		
1	CH3_0-	21	CH4_2+
2	CH3_0+	22	GND
3	CH3_1-	23	CH4_CLK-
4	CH3_1+	24	CH4_CLK+
5	CH3_2-	25	GND
6	CH3_2+	26	CH4_3-
7	GND	27	CH4_3+
8	CH3_CLK-	28	NC
9	CH3_CLK+	29	NC
10	GND	30	NC
11	CH3_3-	31	NC
12	CH3_3+	32	NC
13	NC	33	IMS
14	NC	34	NC
15	GND	35	GND
16	CH4_0-	36	VDD
17	CH4_0+	37	VDD
18	CH4_1-	38	VDD
19	CH4_1+	39	VDD
20	CH4_2-	40	VDD

整机技术要求：

1. 整机表面整洁光滑，不应有凹凸变形、粗糙不平、划伤、间隙、裂纹、毛刺、边缘棱角突出、霉斑、脏污、指纹、色差、螺丝孔堵塞、金属斑点、黑点、纹理等任何缺陷；
2. 所有五金件切口及螺丝沉头位置做防锈处理；
3. 所有装配螺丝孔牙长3.0±0.5mm；
4. 未注尺寸公差参照尺寸公差对应表；

设计			Name:	Liquid Crystal Display	P/N:	DBC220AZN40-30L100A
审核			整机规格:	22 inch	Drawing No.:	
核准			单位	mm	比例	1:1
公差	0~30 ±0.50 >30~100 ±0.80					
	>100 ±1.0 ANGULAR: ± 0.3°					
A4	1rd ANGLE PROJECTION			APTUS INTERNATIONAL CO.,LTD		